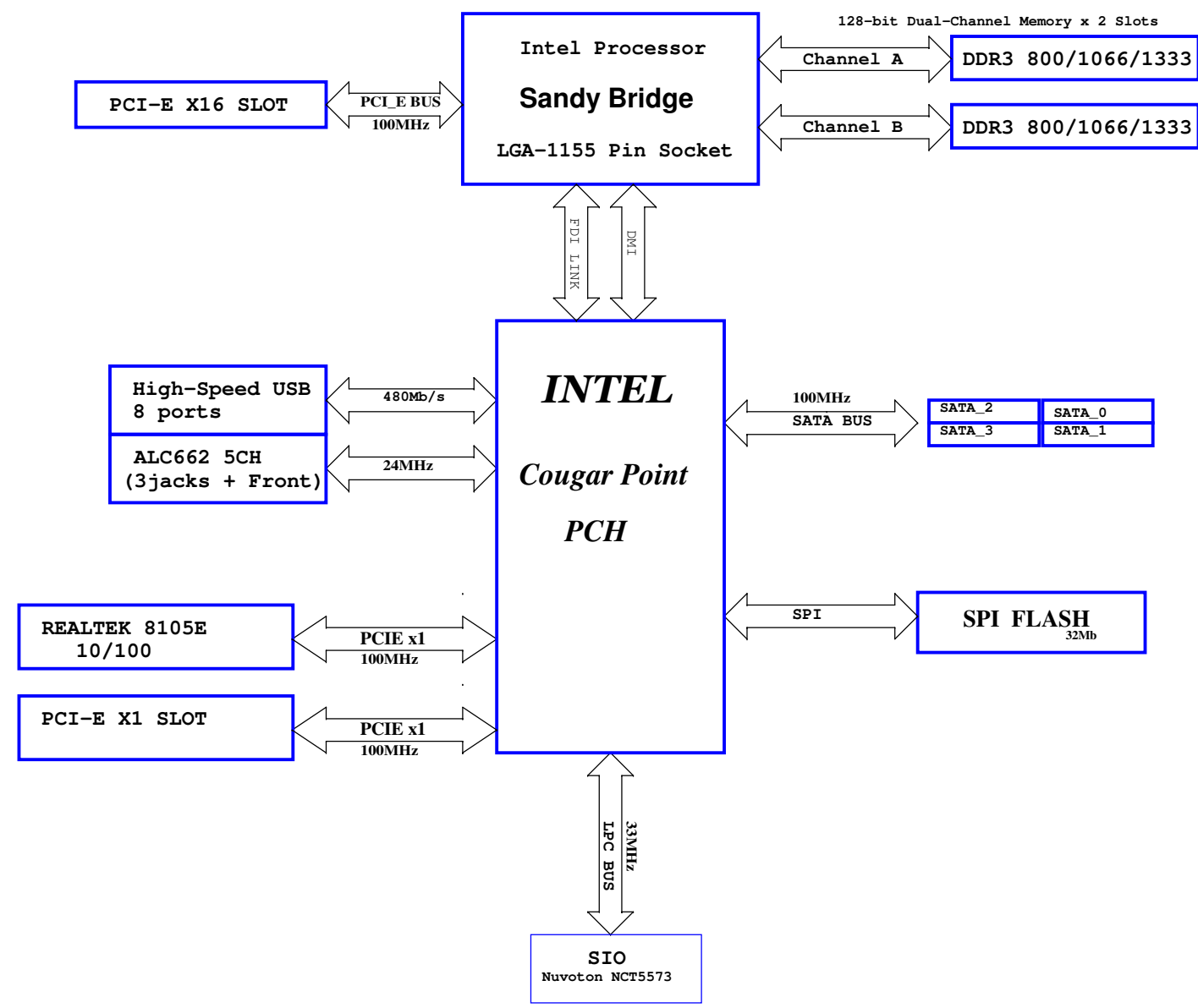


# H61M-VS4 R1.01

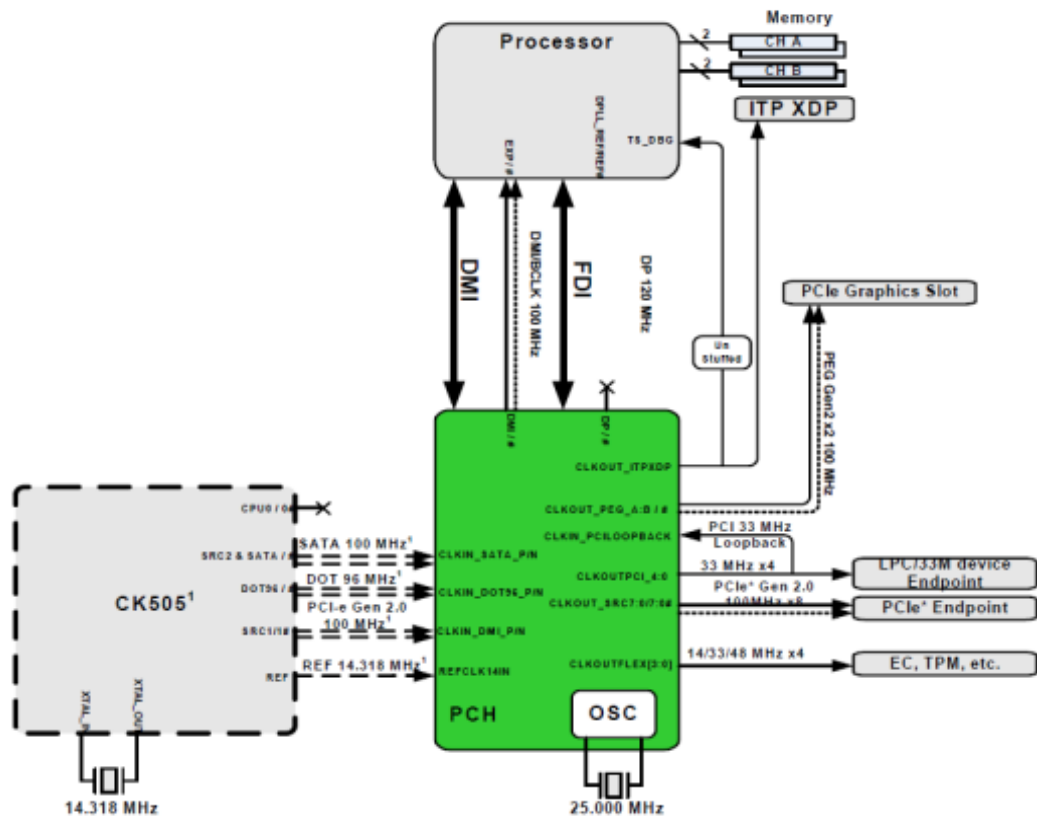
Draft



## Schematics Change History

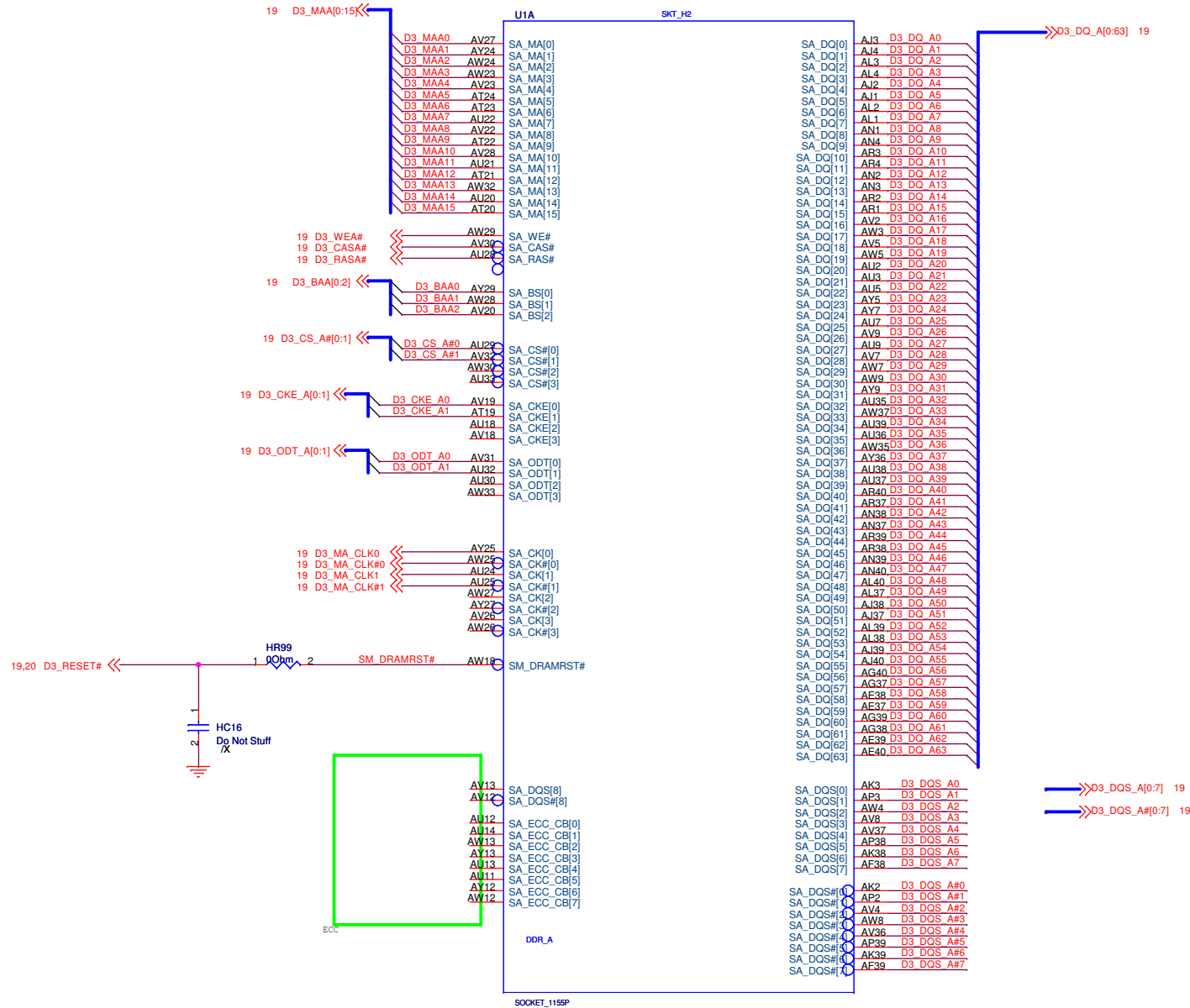
Version	Date	Comments
H61M-VS3 1.00	2012/09/14	Primary release

Full Integrated Clock Mode



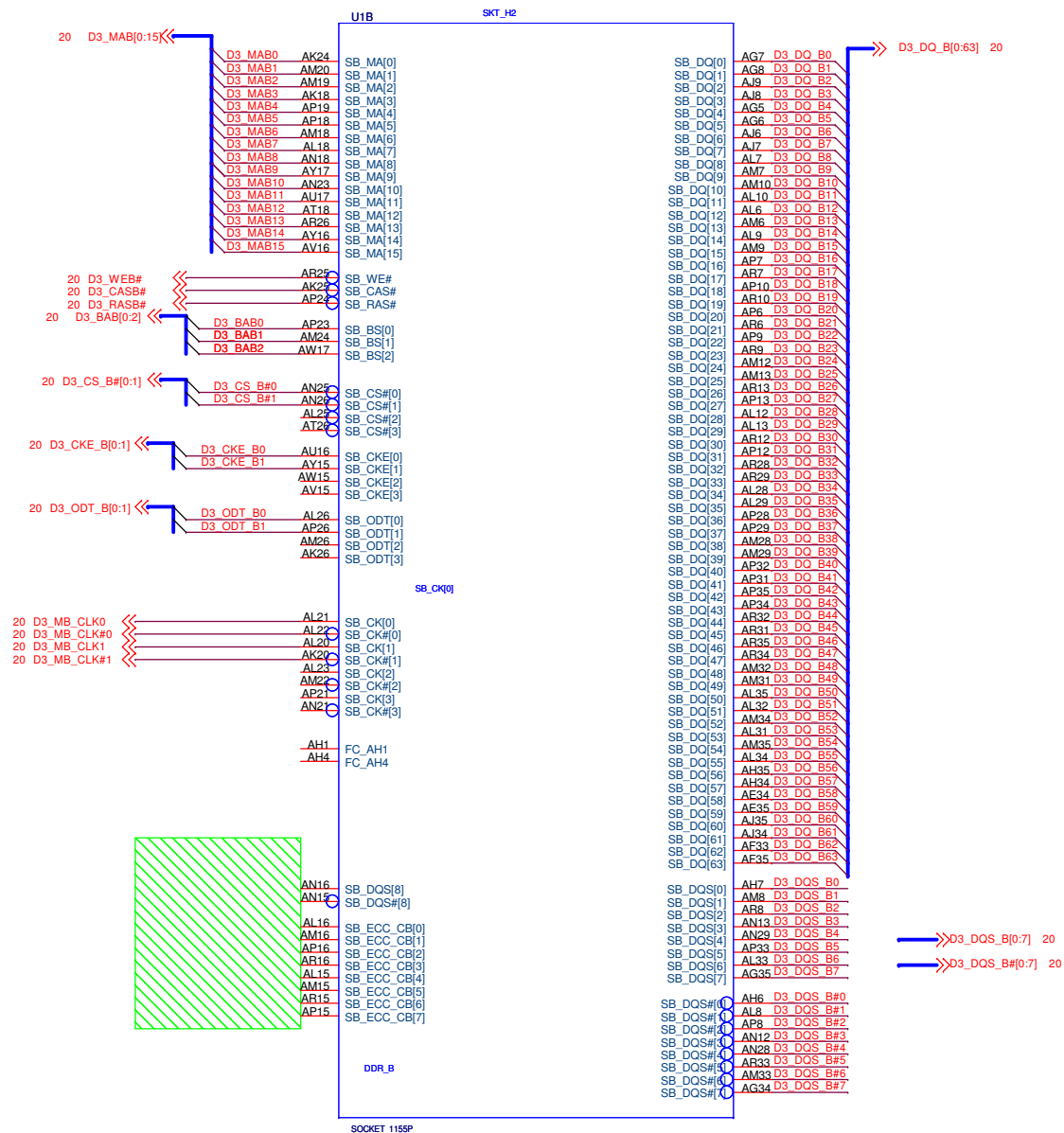
1. CK505 and PCH input clock sources indicated are Buffer Through mode back-up routes only and can be un-stuffed when in full clock integration mode

NO DATA MASK (DM) on Sandy Bridge Memory Controller!  
Tie DM signals to GND in the DIMM side!!

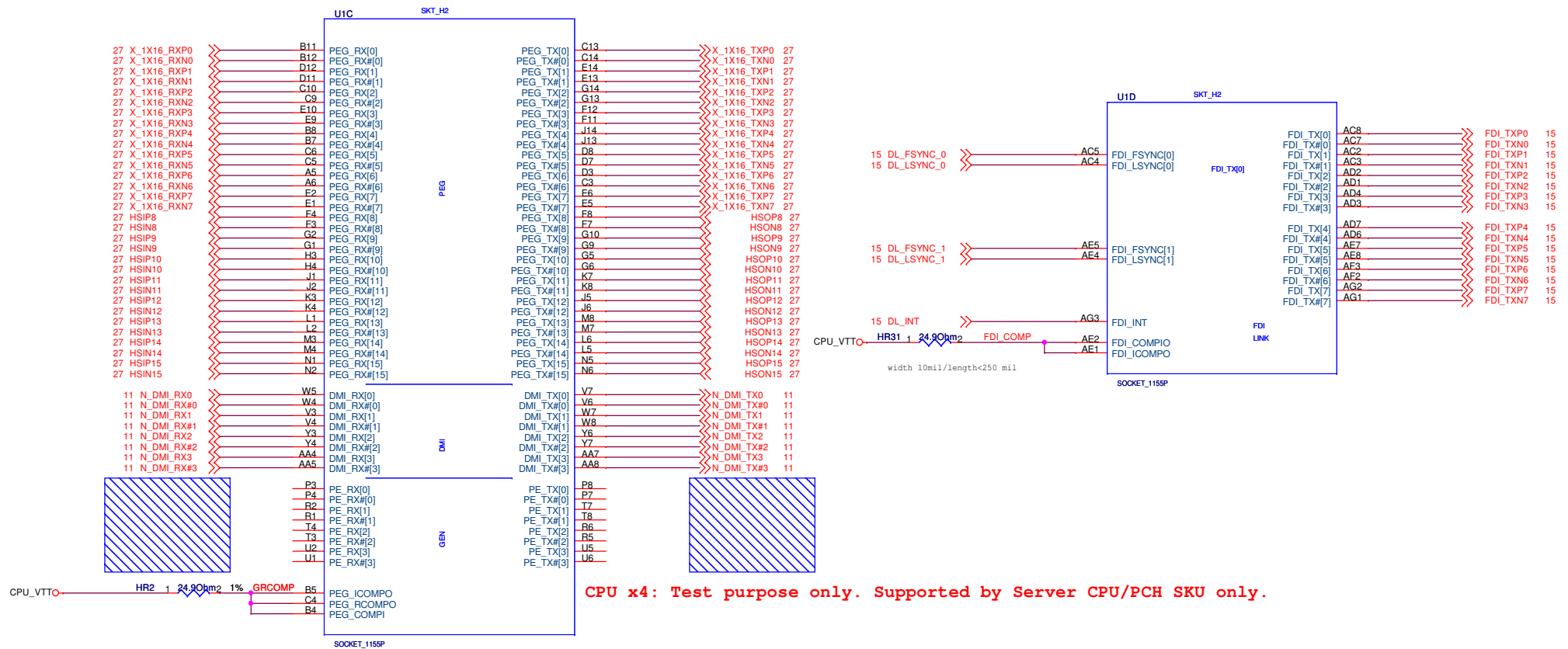


H67M-ITX

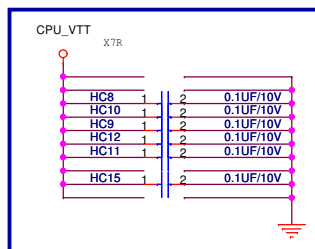
NO DATA MASK (DM) on Sandy Bridge Memory Controller!!  
Tie DM signals to GND in the DIMM side!!



H67M-ПХ



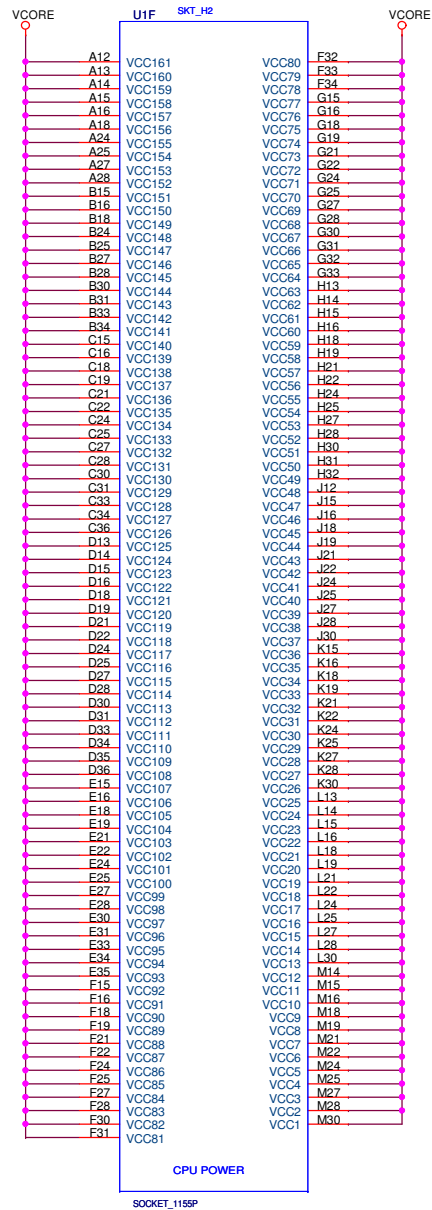
GRCOMP<500mil  
U1.B4 and U1.C4 tight together then use 4 mil trace to HR2.2  
U1.B5 use 10 mil trace separate to HR2.2



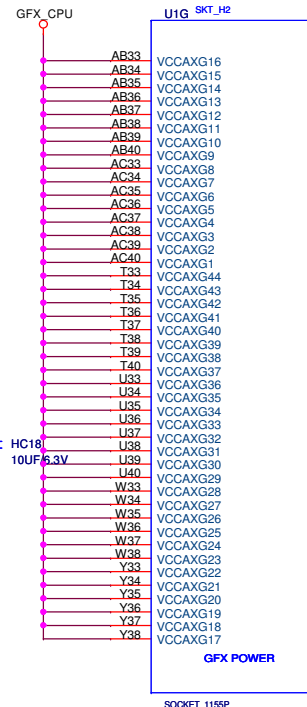
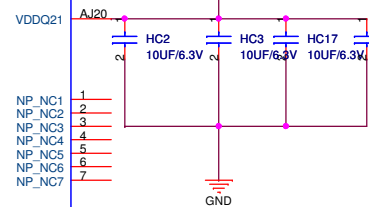
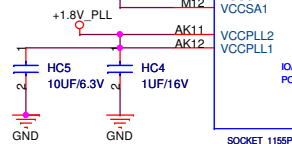
for PCIE signal trans-layer decoupling capacitors!!!  
Place near trans-layer vias for PCIE lanes.

H67M-ITX





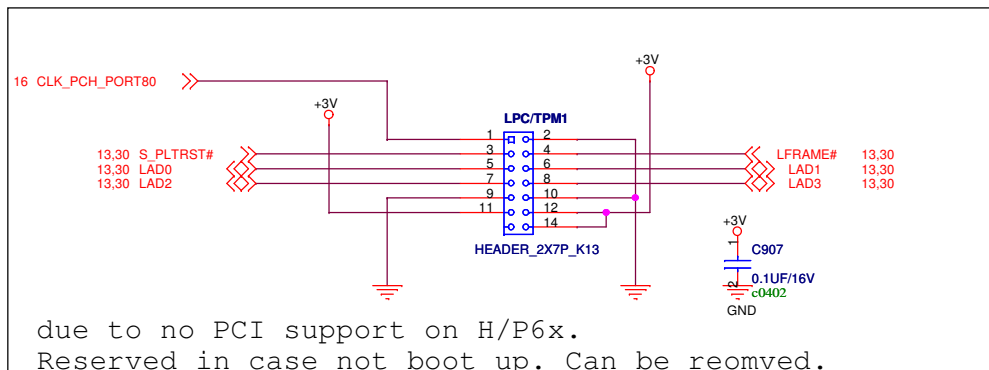
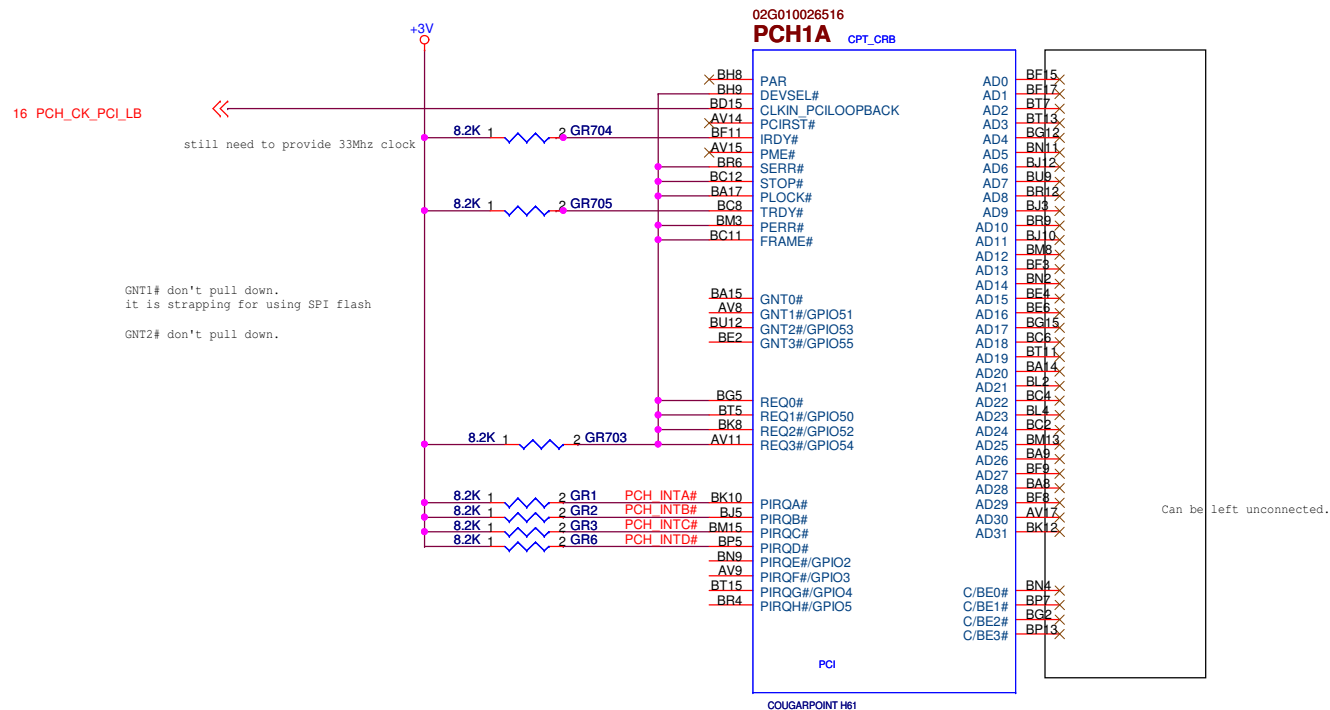
NEW. System Agent Power. (0.85V/0.925V)





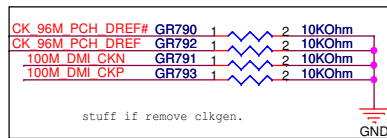


H67/P67 do not support PCI. Check PCI solution!!!



H67M-ITX

		<b>Title :PCH - PCI/LPC</b>	
<b>ASRock Inc.</b>		<b>Engineer: Isaac Lee</b>	
<b>Size B</b>	<b>Project Name H67M-ITX</b>		<b>Rev 1.03</b>
<b>Date: Thursday, March 14, 2013</b>		<b>Sheet 10</b>	<b>of 47</b>

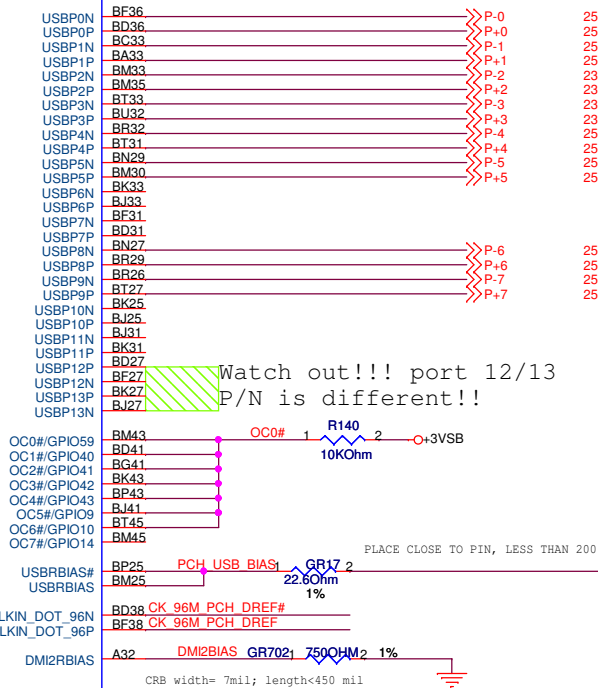


02G010026516  
**PCH1B**

CPT\_CRB



COUGARPOINT H61

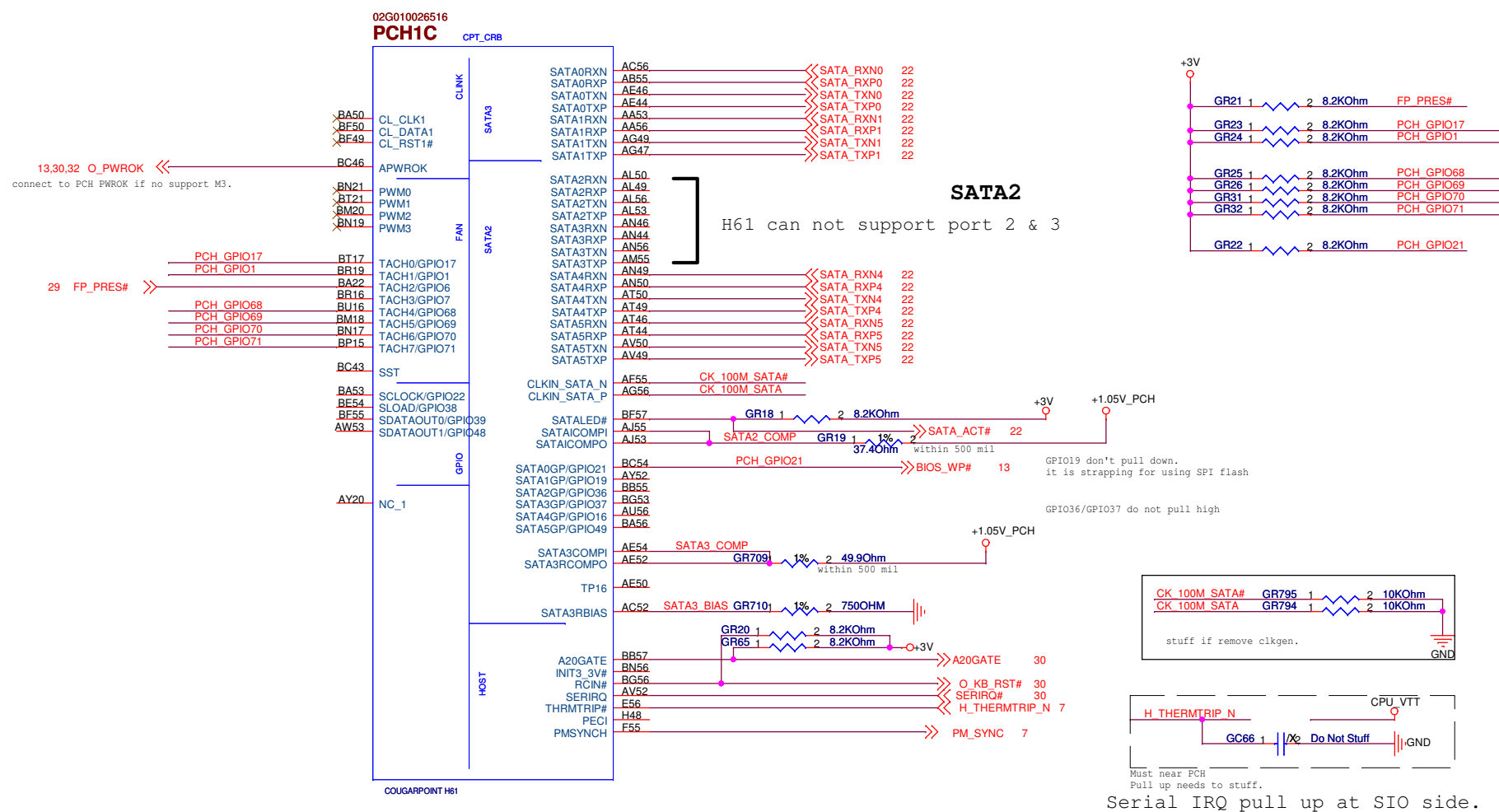


Watch out!!! port 12/13  
P/N is different!!

PLACE CLOSE TO PIN, LESS THAN 200 MILS. Width = 4 mil

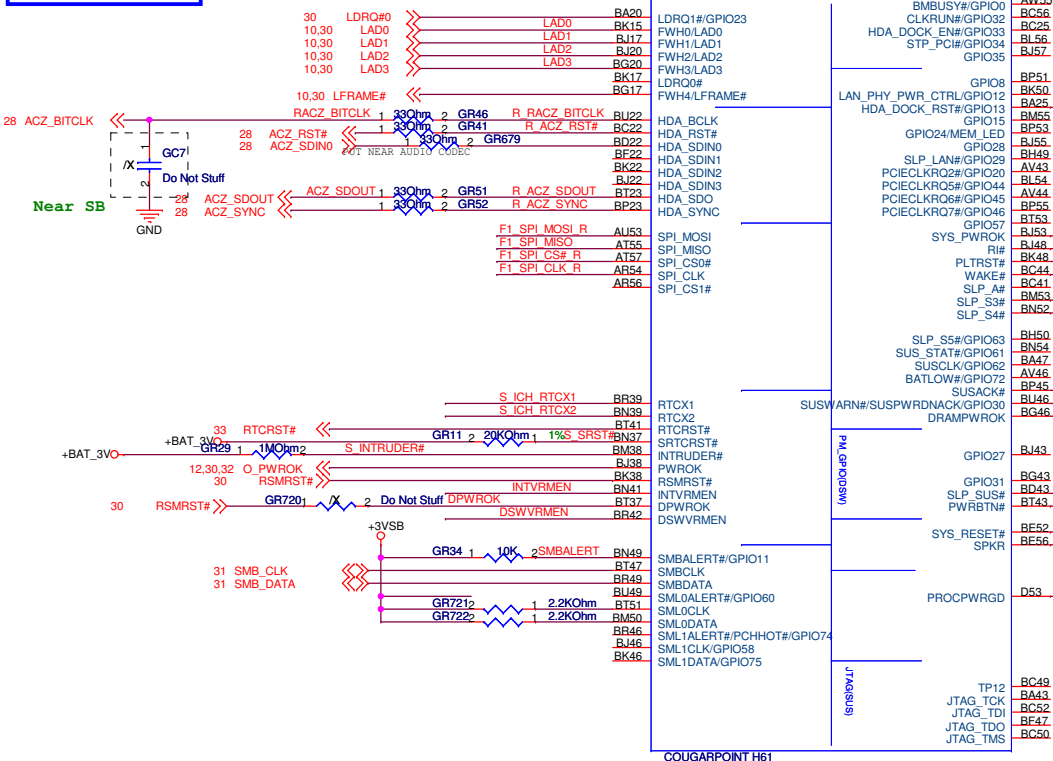
H67M-ITX

<b>ASRock</b>		<b>Title :PCH - PCIE/DMI/USB</b>	
ASRock Inc.		Engineer: <b>Isaac Lee</b>	
Size <b>B</b>	Project Name <b>H67M-ITX</b>		Rev <b>1.03</b>
Date: <b>Thursday, March 14, 2013</b>		Sheet <b>11</b> of <b>47</b>	



GPIO28	High
HDA_SYNC	Low

**PCH1D**



DSIVVRMEN GR729: 1 392KOhm  
INTVRMEN GR33: 2 392KOhm

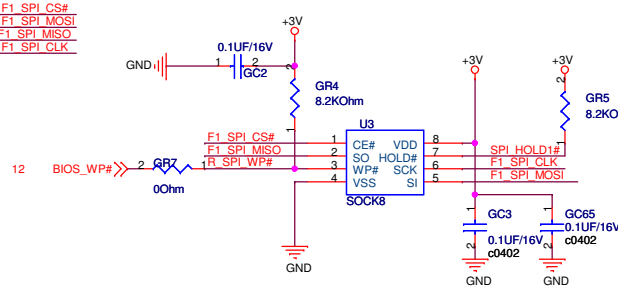
PWM PG 0.1UF/16V 2 1 GC63  
RSMRST: 0.022UF/16V 2 1 GC64  
O PWROK GR732: 1 10KOhm  
R ACZ SYNC GR727: 2 1KOhm

[illegible]

U3\_1

SPI

32M

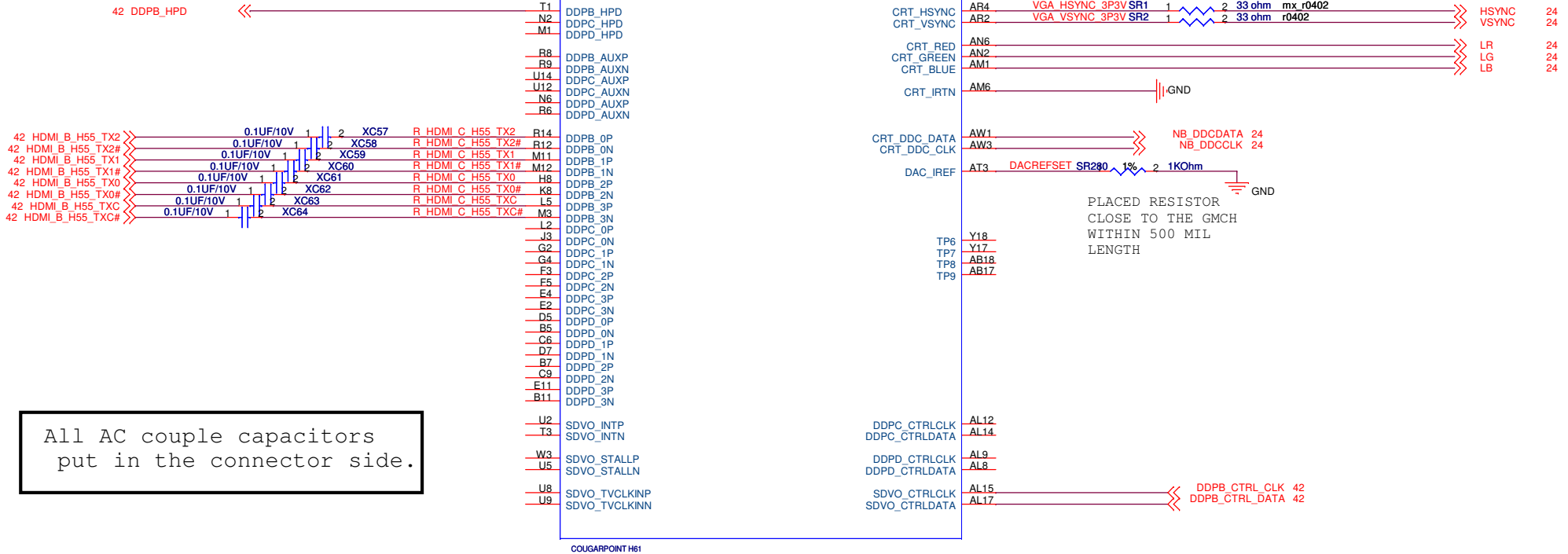


Schematic diagram of a 32.768KHz crystal oscillator circuit. The circuit includes a crystal (GY1, 32.768KHZ), two capacitors (GC5, GC6, 10PF/50V), and a 10MOhm resistor (GR14). It is powered by S\_I2C1\_RTCX1 and S\_I2C1\_RTCX2, and its output is connected to S\_SRST#. The diagram also shows ground connections and a jumper wire (GY1\_1) with dimensions 0.5\*6.3\*4\*6.3mm.

		<b>Title :</b> Audio/MISC	
<b>ASRock Inc.</b>		<b>Engineer:</b> Isaac Lee	
Size Custom	Project Name <b>H67M-ITX</b>		Rev 1.03
Date: Friday, March 15, 2013		Sheet 13 of 47	

02G010026516  
**PCH1F**

CPT\_CRB




All AC couple capacitors  
put in the connector side.

- In an effort to address customer display issues more efficiently Intel recommends customers adopt digital display configuration similar to Intel CRB as following

Digital Port	Display Technology
Port B	DVI or SDVO (Desktop) DisplayPort, HDMI/DVI or SDVO (Mobile)
Port C	DisplayPort (Desktop) DisplayPort/HDMI/DVI (Mobile)
Port D	HDMI/DVI/eDP* (Desktop) HDMI/DVI/DisplayPort (Mobile)

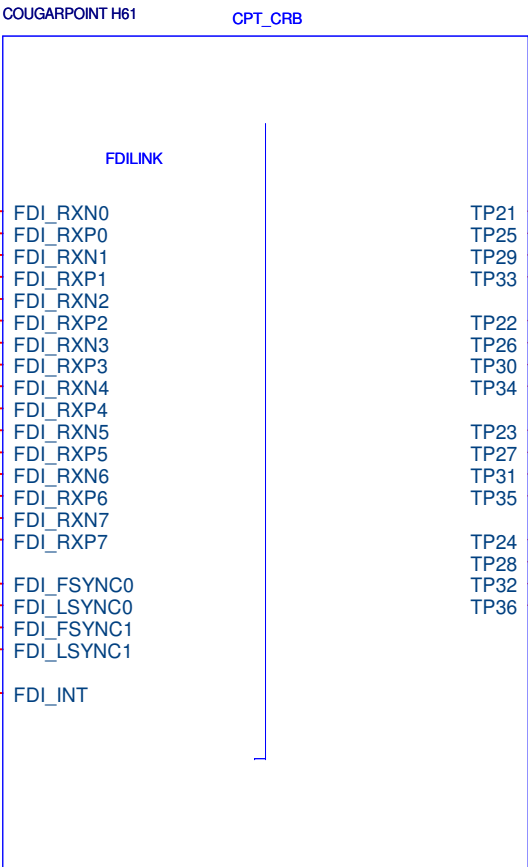
H67M-ITX

		Title :PCH - Display	
ASRock Inc.		Engineer: Isaac Lee	
Size B	Project Name <b>H67M-ITX</b>		Rev 1.03
Date: Thursday, March 14, 2013	Sheet 14	of 47	

6 FDI\_TXN0  
6 FDI\_TXP0  
6 FDI\_TXN1  
6 FDI\_TXP1  
6 FDI\_TXN2  
6 FDI\_TXP2  
6 FDI\_TXN3  
6 FDI\_TXP3  
6 FDI\_TXN4  
6 FDI\_TXP4  
6 FDI\_TXN5  
6 FDI\_TXP5  
6 FDI\_TXN6  
6 FDI\_TXP6  
6 FDI\_TXN7  
6 FDI\_TXP7  
  
6 DL\_FSYNC\_0  
6 DL\_LSYNC\_0  
6 DL\_FSYNC\_1  
6 DL\_LSYNC\_1  
  
6 DL\_INT




C42  
B43  
F45  
F43  
H41  
J41  
C46  
D47  
B45  
A46  
B47  
C49  
J43  
H43  
M43  
P43  
  
B51  
E49  
C52  
D51  
  
H46



PCH1G  
02G010026516

TP21 H31  
TP25 J31  
TP29 C29  
TP33 E29  
  
TP22 J27  
TP26 L27  
TP30 F28  
TP34 E27  
  
TP23 J25  
TP27 L25  
TP31 C26  
TP35 B27  
  
TP24 L22  
TP28 J22  
TP32 B25  
TP36 D25

H67M-ITX

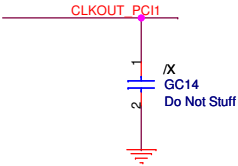
			Title : PCH - FDI		
ASRock Inc.			Engineer: Isaac Lee		
Size A	Project Name H67M-ITX				Rev 1.03
Date: Thursday, March 14, 2013			Sheet 15 of 47		

**FLEX CLK HAS RULE OF USING.  
SEE PDG PAGE 191 FOR DETAILS.**

02G010026516  
**PCH1H**

CPT\_CRB

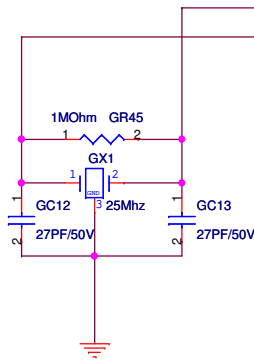
30 PCH\_CK\_33M\_SIO >> GR736 1 2 220hm AT11  
10 CLK\_PCH\_PORT80 >> GR773 1 2 220hm CLKOUT\_PCH1 AN14  
10 PCH\_CK\_PCL\_LB << GR770 1 2 220hm AT12



23 PCH\_25M >> RG31 1 2 00hm LAN\_25M AW5  
30 PCH\_CK\_48M\_SIO >> BA2  
+1.05V\_PCH\_O 90.90hm 2 1% 1 GR43 AL2

14Mhz no need to connect by using internal clock.

Flex 0, 1, 2, 3 : Check ME setting!!



AT9 CLKOUTFLEX0/GPIO64  
BA5 CLKOUTFLEX1/GPIO65  
AW5 CLKOUTFLEX2/GPIO66  
BA2 CLKOUTFLEX3/GPIO67

AL2 XCLK\_RCOMP  
AN8 REFCLK14IN



AJ5 XTAL25\_OUT  
AJ3 XTAL25\_IN

COUGARPOINT H61

CLKIN\_GND1\_N R27  
CLKIN\_GND1\_P P27  
CLKIN\_GND0\_N W53  
CLKIN\_GND0\_P V52  
CLKOUT\_ITPXD\_P N52  
CLKOUT\_ITPXD\_P N52  
CLKOUT\_PCIE7N AE2  
CLKOUT\_PCIE7P AF1  
CLKOUT\_DMI\_N P31  
CLKOUT\_DMI\_P R31  
CLKOUT\_DP\_N N56  
CLKOUT\_DP\_P M55  
CLKOUT\_PCIE0N AE6  
CLKOUT\_PCIE0P AC6  
CLKOUT\_PCIE1N AA5  
CLKOUT\_PCIE1P W5  
CLKOUT\_PCIE2N AB12  
CLKOUT\_PCIE2P AB14  
CLKOUT\_PCIE3N AB9  
CLKOUT\_PCIE3P AB8  
CLKOUT\_PCIE4N Y9  
CLKOUT\_PCIE4P Y8  
CLKOUT\_PCIE5N AF3  
CLKOUT\_PCIE5P AG2  
CLKOUT\_PCIE6N AB3  
CLKOUT\_PCIE6P AA2  
CLKOUT\_PEG\_A\_N AG8  
CLKOUT\_PEG\_A\_P AG9  
CLKOUT\_PEG\_B\_N AE12  
CLKOUT\_PEG\_B\_P AE11




CPU

PCIE x1 Slot

LAN

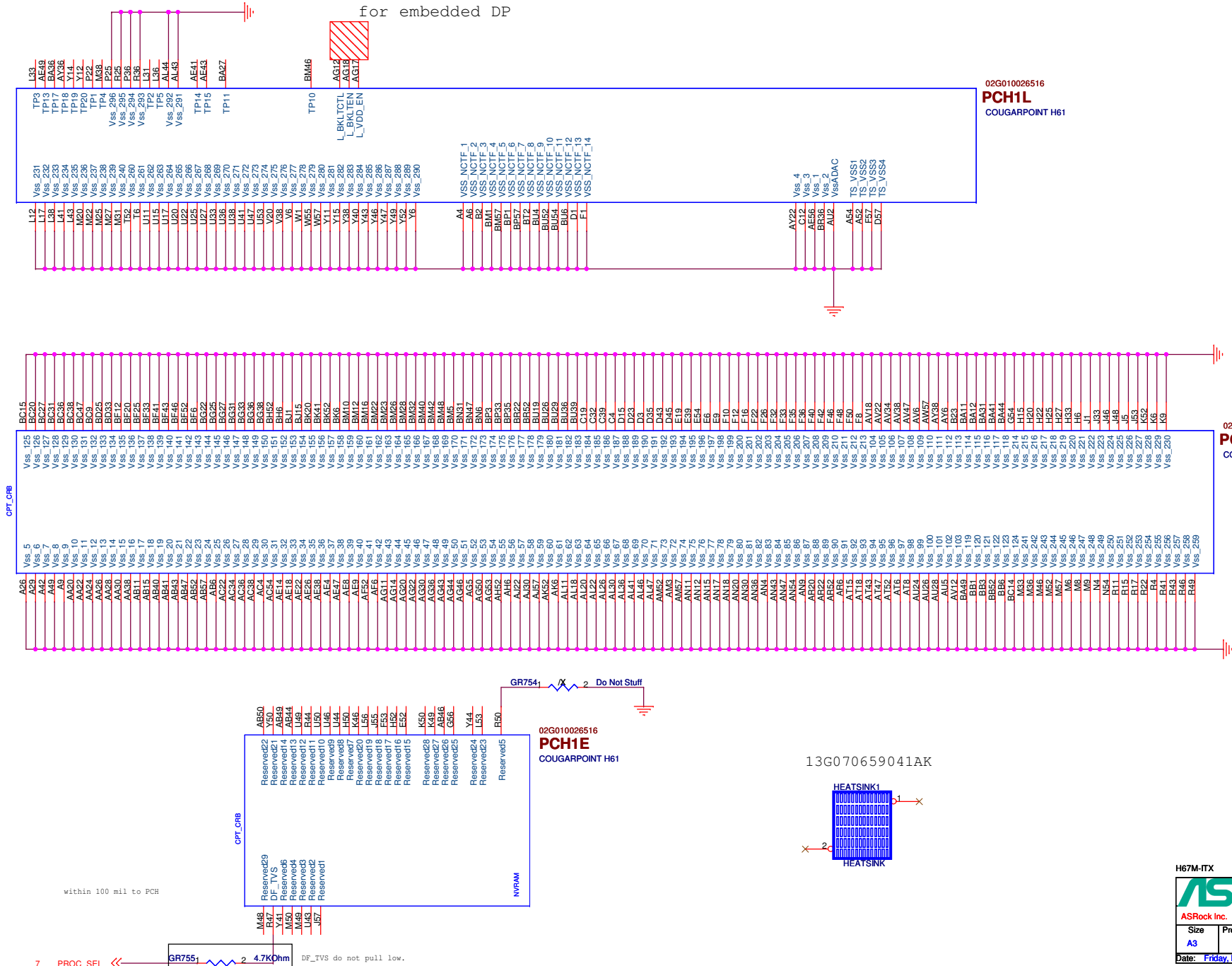
PCIE x16 Slot

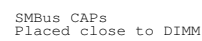
H67M-ITX

		Title :PCH - CLK	
ASRock Inc.		Engineer: Isaac Lee	
Size B	Project Name H67M-ITX		Rev 1.03
Date: Friday, March 15, 2013		Sheet 16	of 47





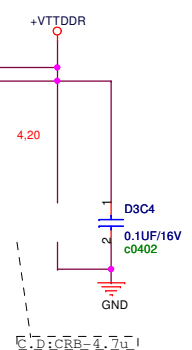


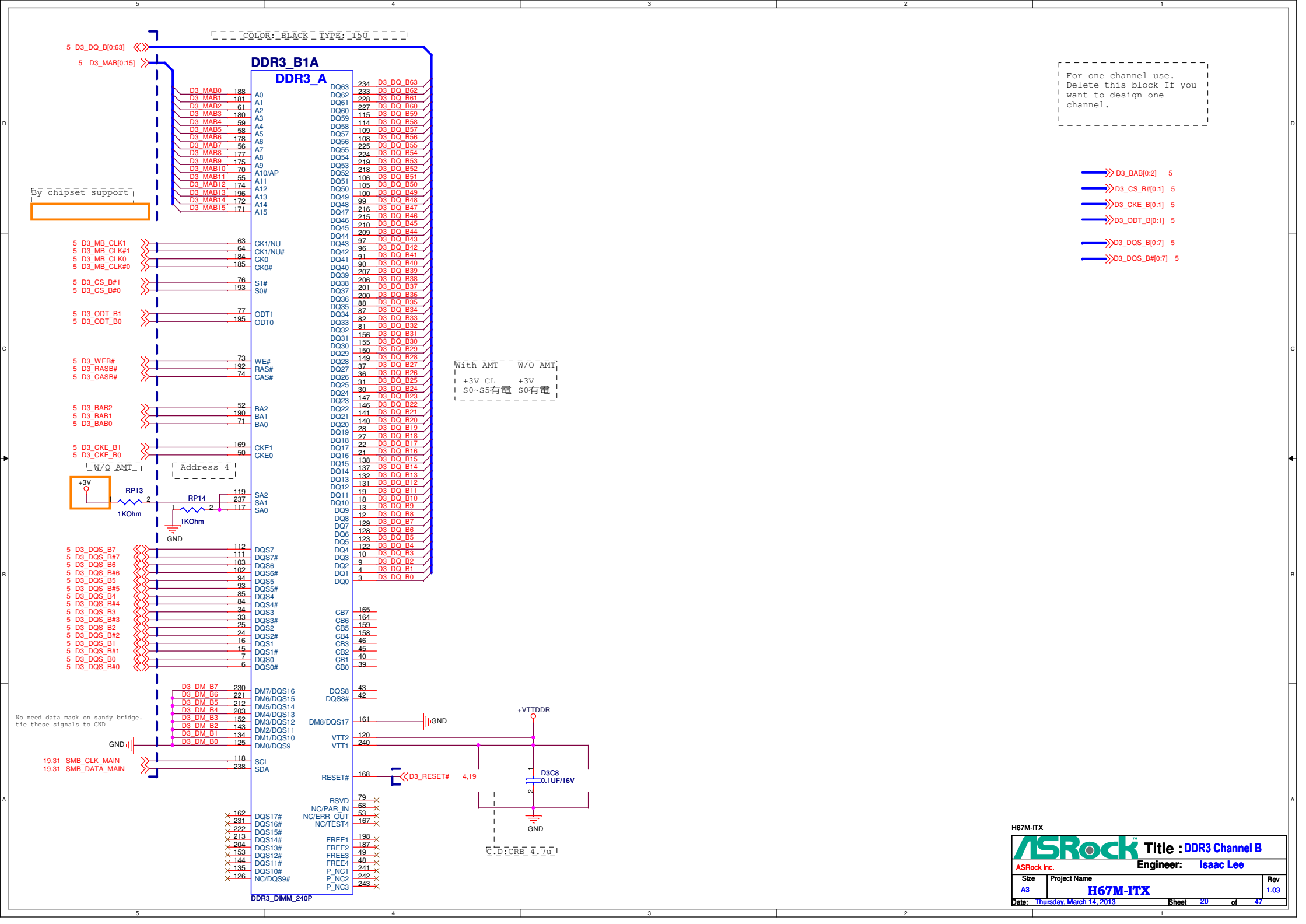


With AMT	W/O AMT
+3V_CL	+3V
S0~S5有電	S0有電

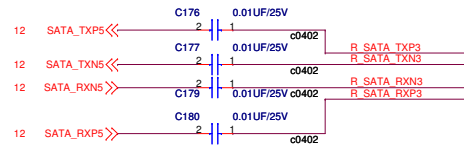
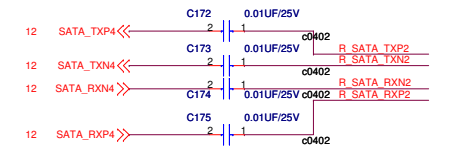
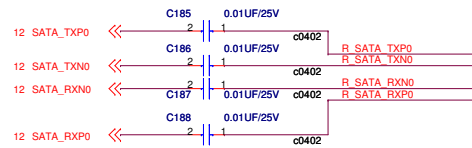
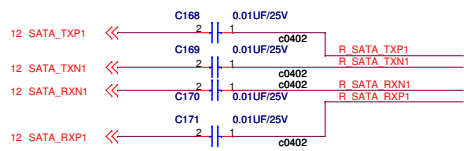
Supported ECC<sub>1</sub>

No need data mask on sandy bridge.  
tie these signals to GND



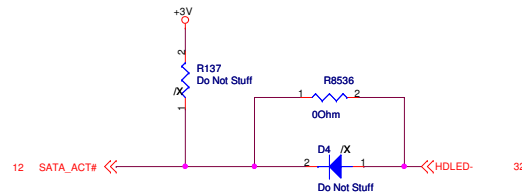




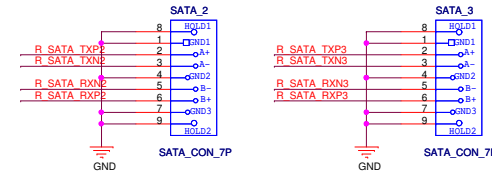


## SATA3 & SATA LED

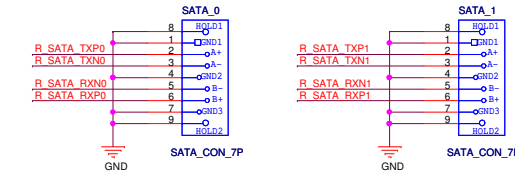
1.00 Internal Pull UP  
1.00 If need pul up,  
check +3.3V or +5V



## INTEL SATA2



## INTEL SATA3

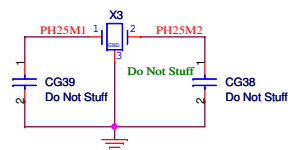
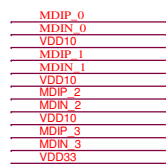
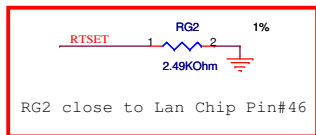
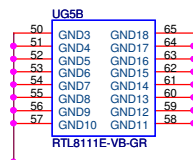
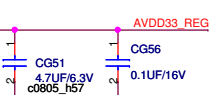
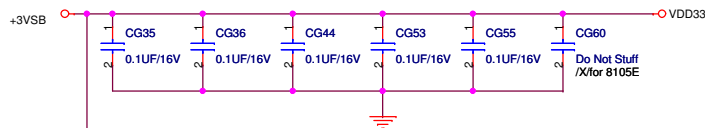


Check SATA Port Name with leaders!!!

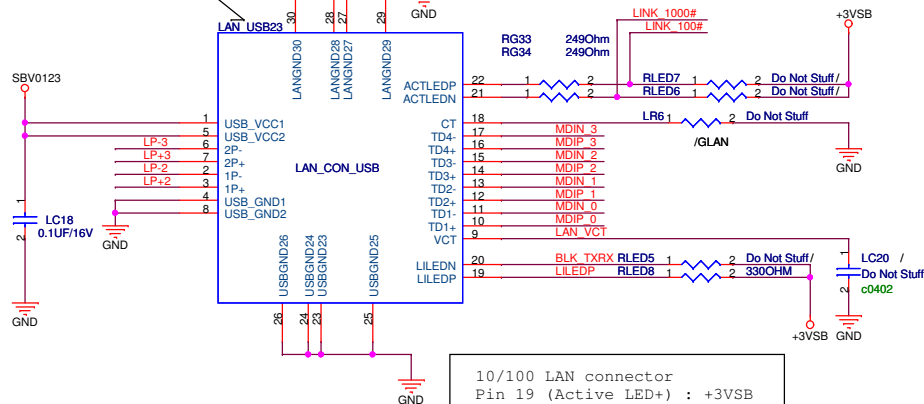
H67M-ITX

<b>ASRock</b>		Title : <b>SATA3/SATA2 / ESATA</b>	
ASRock Inc.		Engineer: <b>Isaac Lee</b>	
Size	Project Name	Rev	
Custom	<b>H67M-ITX</b>	1.03	
Date: Friday, March 15, 2013	Sheet 22	of 47	

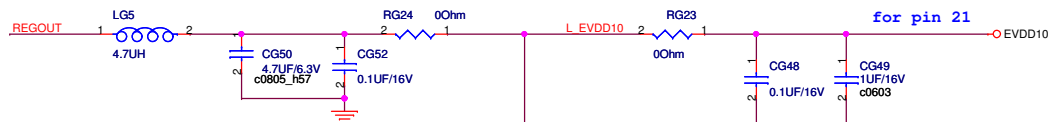
pin12,27,39,42,47,48 for RTL8111E  
pin27,39,42,47,48 for RTL8105E



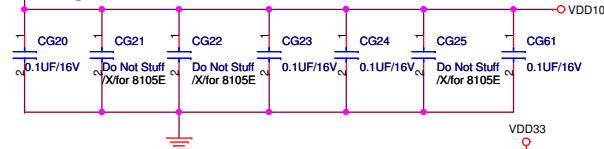
LAN\_USB01 P/R:  
10/100: 12G142333224  
1000 : 12G14263322WAK



10/100 LAN connector  
Pin 19 (Active LED+) : +3VSB  
Pin 20 (Active LED-) : LED3  
Pin 21 (Link LED+) : LED0  
Pin 22 (Link LED-) : LED1

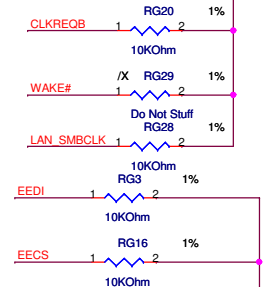


pin3,6,9,13,29,41,45 for RTL8111E  
pin3,13,29,45 for RTL8105E



When using EFUSE/BIOS patch without ASF function

Enable Switch regulator



LED3 for Activity  
LED0,1 for link

Close to Lan Chip

HSIP HSIN

EXP\_TLANN EXP\_TLANN

EXP\_RLANN EXP\_RLANN

PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

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PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

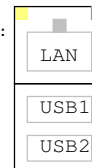
PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

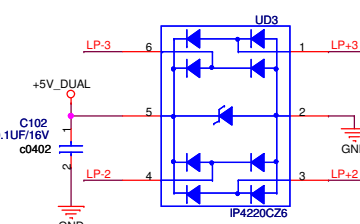
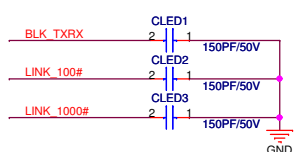
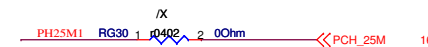
PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

PCH\_ECLK\_LAN# PCH\_ECLK\_LAN#

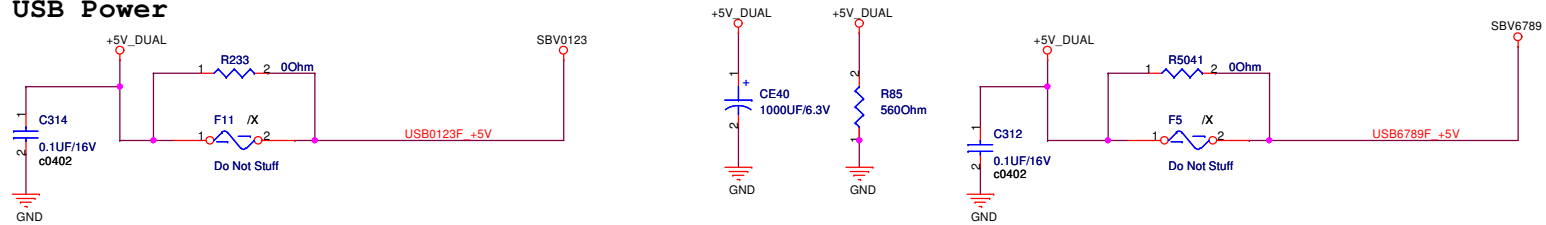
Left LED:  
1. YELLOW :  
Activity



Right LED:  
1. Green : 100Mbps  
2. No Light : 10Mbps



## USB Power

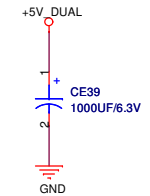
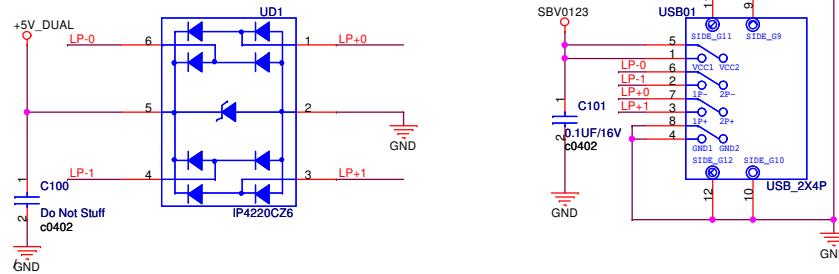


## USB 0, 1

11  
11  
11  
11

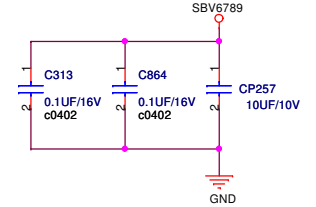
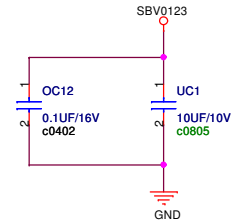
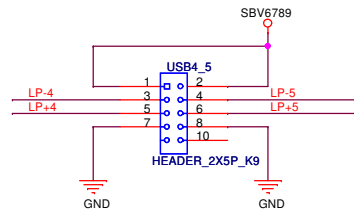
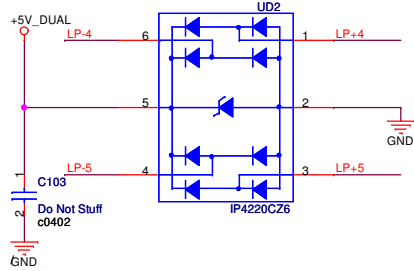
P-1  
P-0  
P+1  
P+0

LP+0 P+0  
LP-0 P-0  
LP+1 P+1  
LP-1 P-1



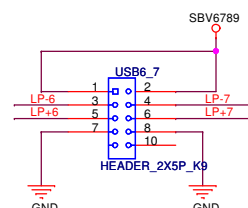
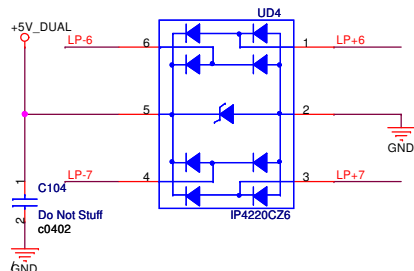
## USB 4, 5

11 P+4 LP+4  
11 P-4 LP-4  
11 P+5 LP+5  
11 P-5 LP-5



## USB 6, 7

11 P+6 LP+6  
11 P-6 LP-6  
11 P+7 LP+7  
11 P-7 LP-7



H67M-ITX

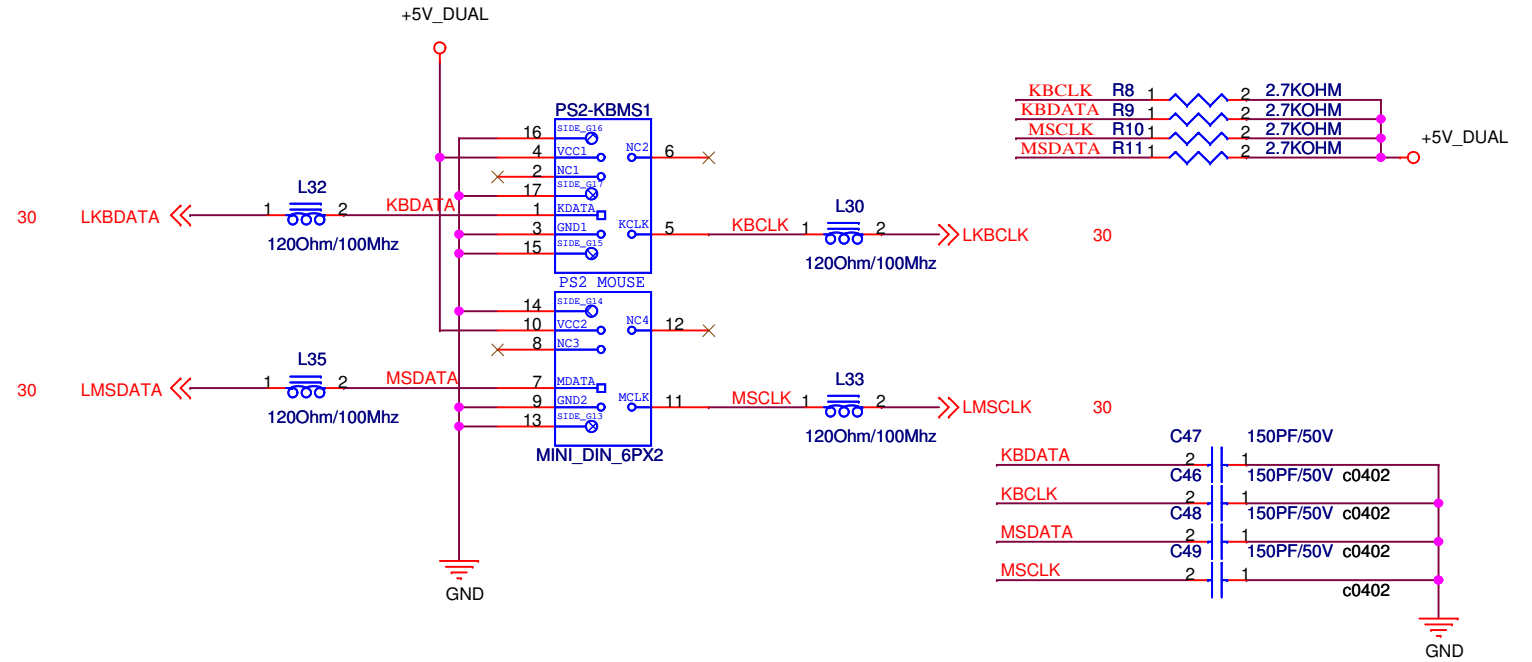
<b>ASRock</b>		<b>Title : USB Port</b>	
ASRock Inc.		<b>Engineer: Isaac Lee</b>	
Size A3	Project Name <b>H67M-ITX</b>	Rev 1.03	
Date: Friday, March 15, 2013		Sheet 25 of 47	

remove ESD protection diode for ON/OFF charge circuit. (to gain more space)

remove ESD protection diode for ON/OFF charge circuit. (to gain more space)



\*Modify LMSCLK & LKBDATA



H67M-ITX

<b>ASRock</b>		Title : <b>KB &amp; MS</b>	
ASRock Inc.		Engineer: <b>Isaac Lee</b>	
Size <b>A4</b>	Project Name <b>H67M-ITX</b>		Rev <b>1.03</b>
Date: <b>Thursday, March 14, 2013</b>		Sheet <b>26</b>	of <b>47</b>

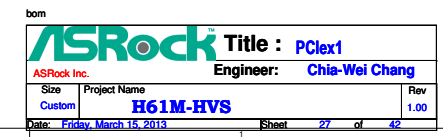
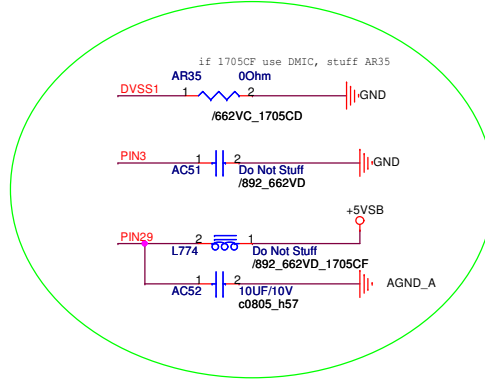
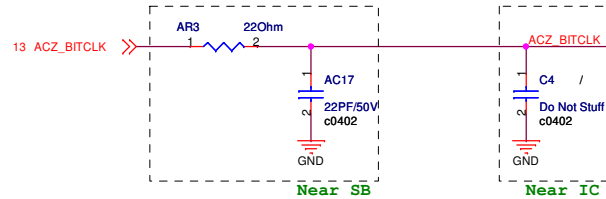
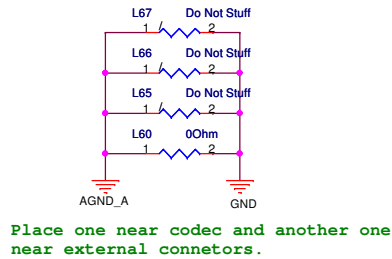
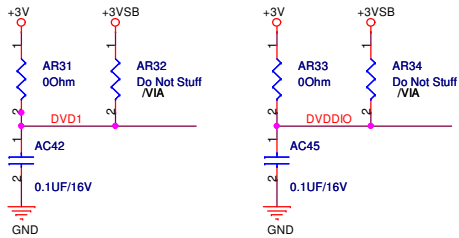
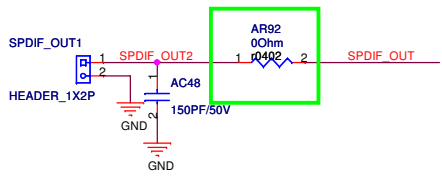
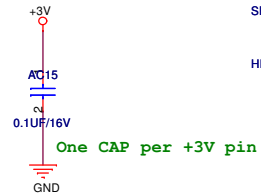


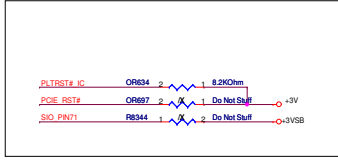
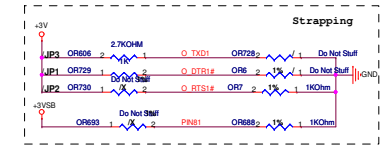
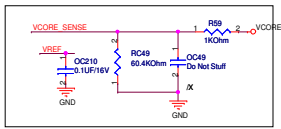
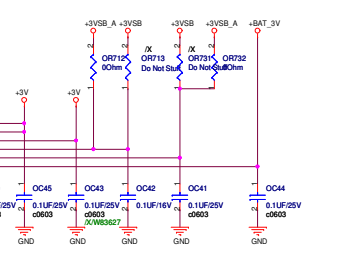
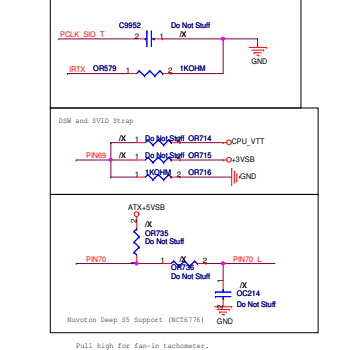
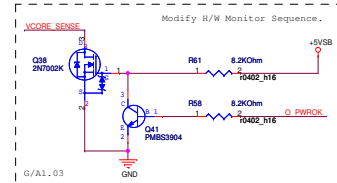
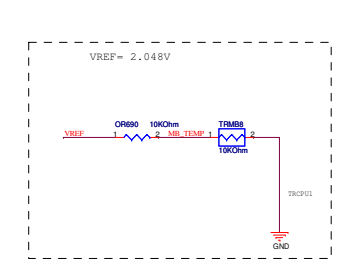
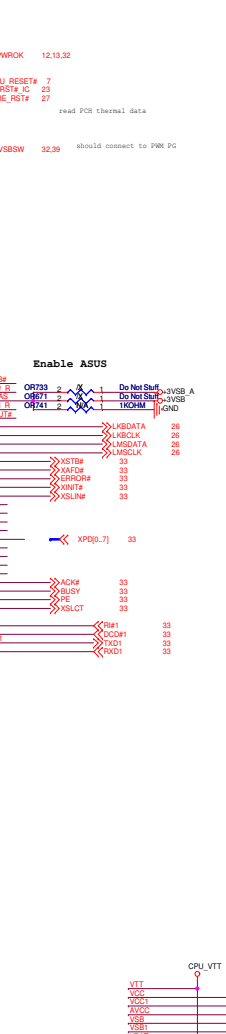
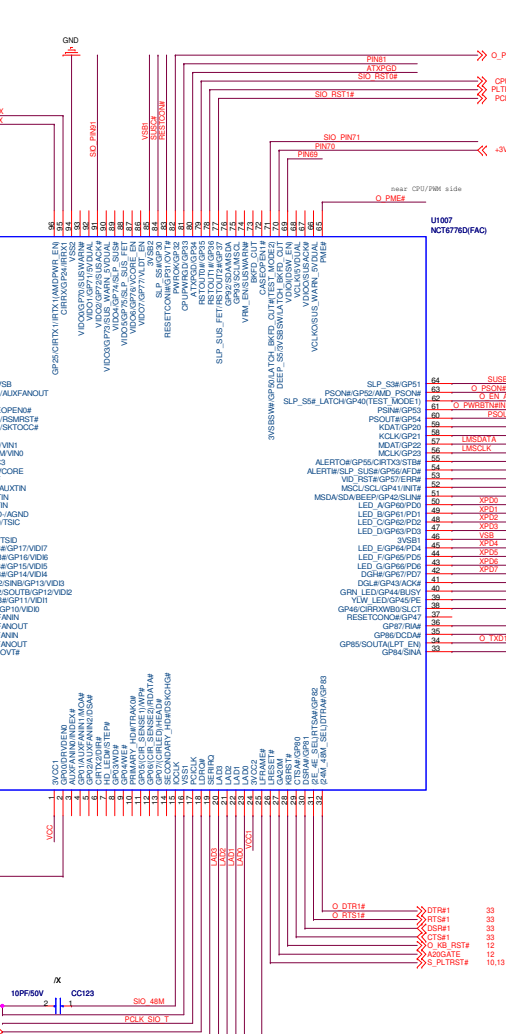
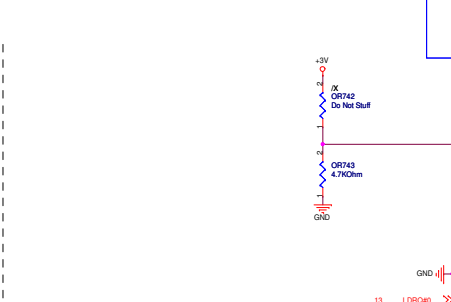
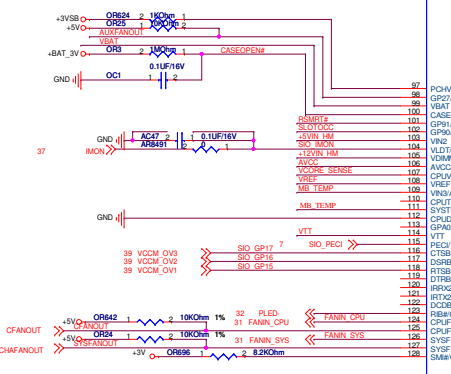
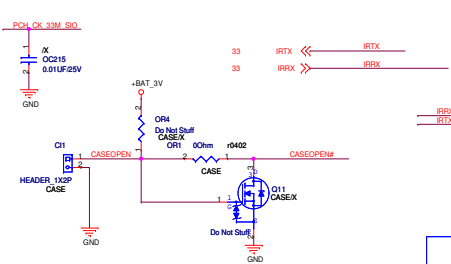
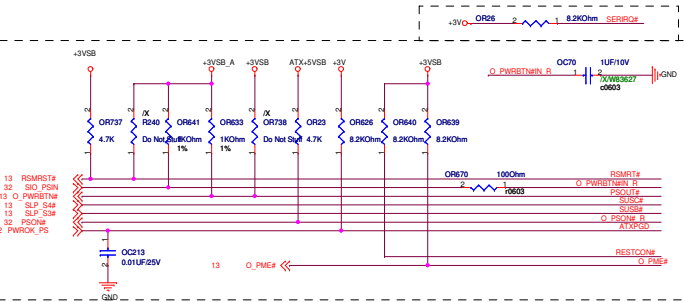
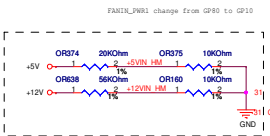
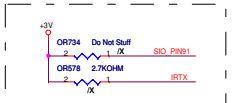
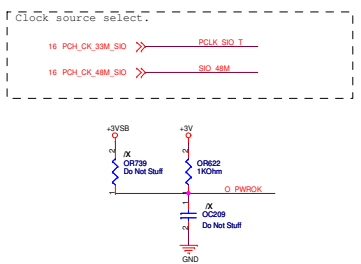
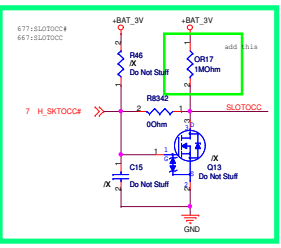
Table 1.

	AR1
662VC/662VD/892/887/1705CF	20K Ohm
VT1705CD/1718/1708	5.1K Ohm



bom



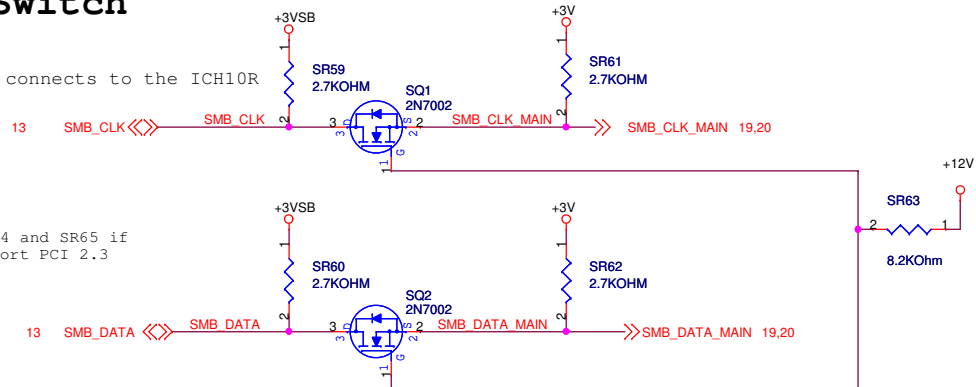


## SMBus Switch

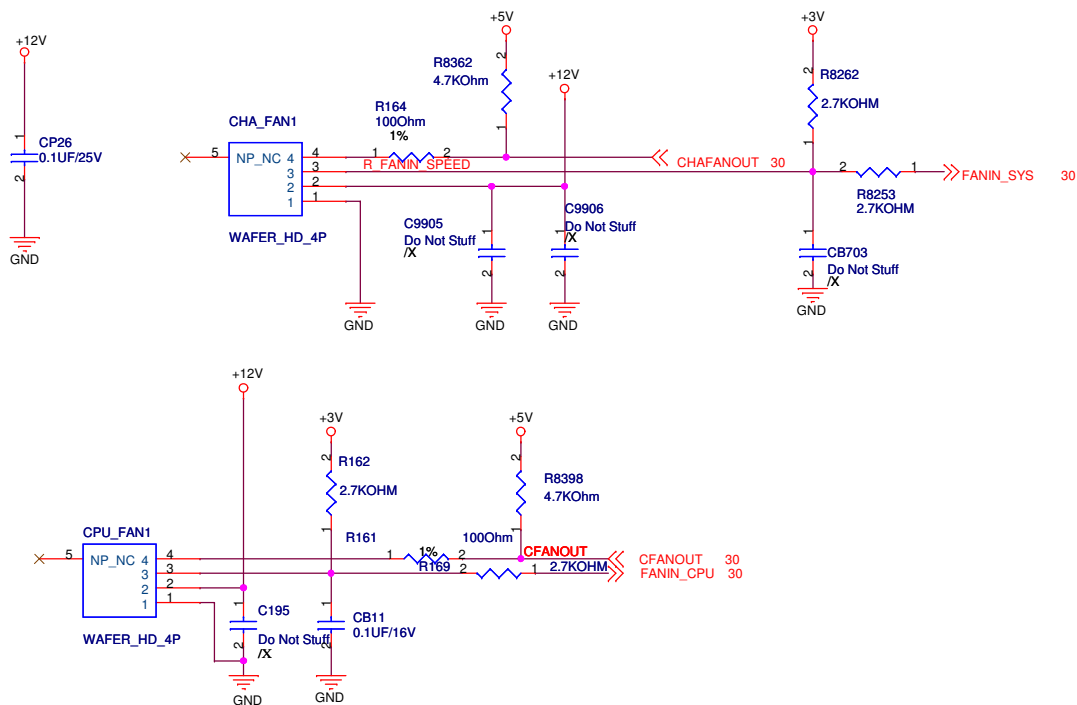
1.00 SMBus connect to two kind of devices, one use Main power, another use Standby power, so use this switch circuit to isolate those two device.  
SMB\_CLK and SMB\_DATA for Standby device.  
SMB\_CLK\_MAIN and SMB\_DATA\_MAIN for Main power device.

SMB\_CLK and SMB\_DATA connects to the ICH10R


Mount those SR64 and SR65 if we want to support PCI 2.3



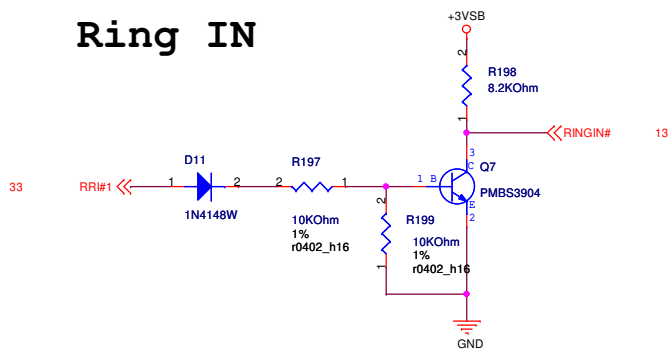
SMB\_CLK\_PCI and SMB\_DATA\_PCI connects to the PCIE slot



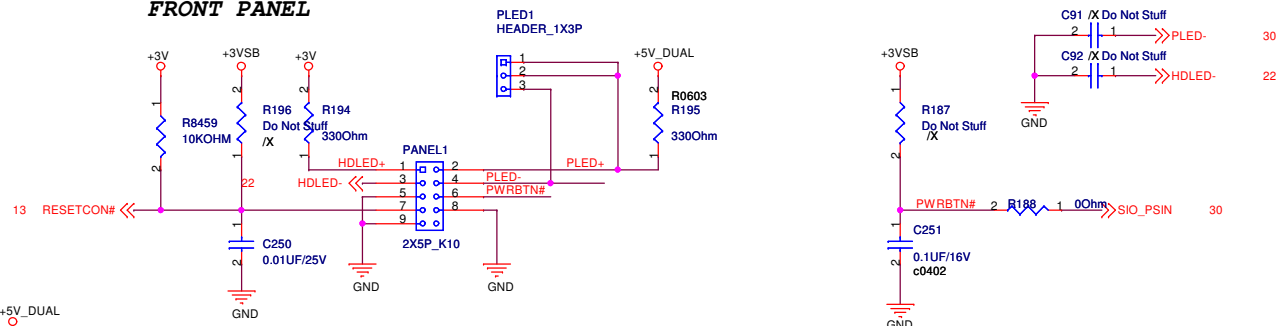
H67M-ITX

		Title : <b>SMBUS SWITCH,FAN</b>	
ASRock Inc.		Engineer: <b>Isaac Lee</b>	
Size <b>B</b>	Project Name <b>H67M-ITX</b>		Rev <b>1.03</b>
Date: <b>Friday, March 15, 2013</b>		Sheet <b>31</b> of <b>47</b>	

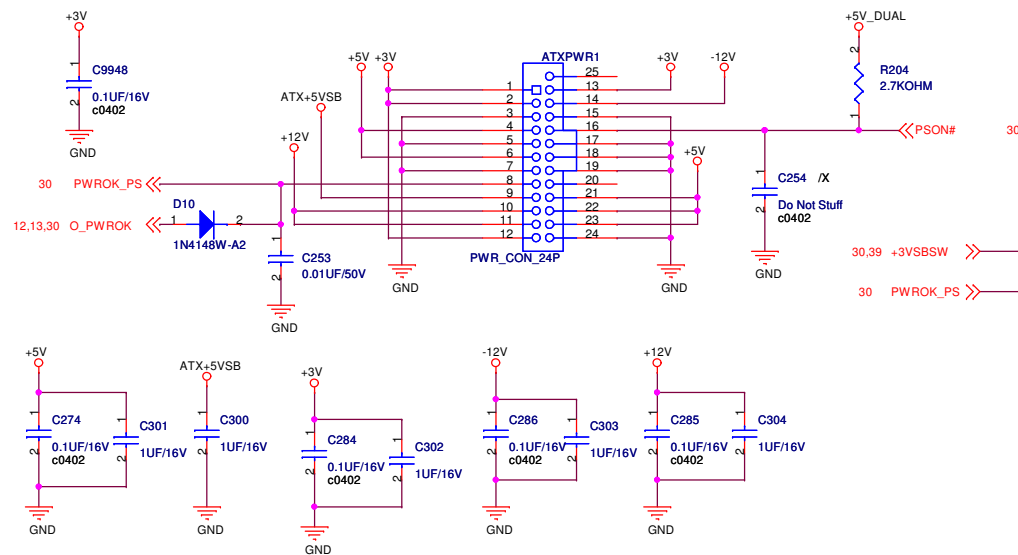
# Ring IN



## FRONT PANEL

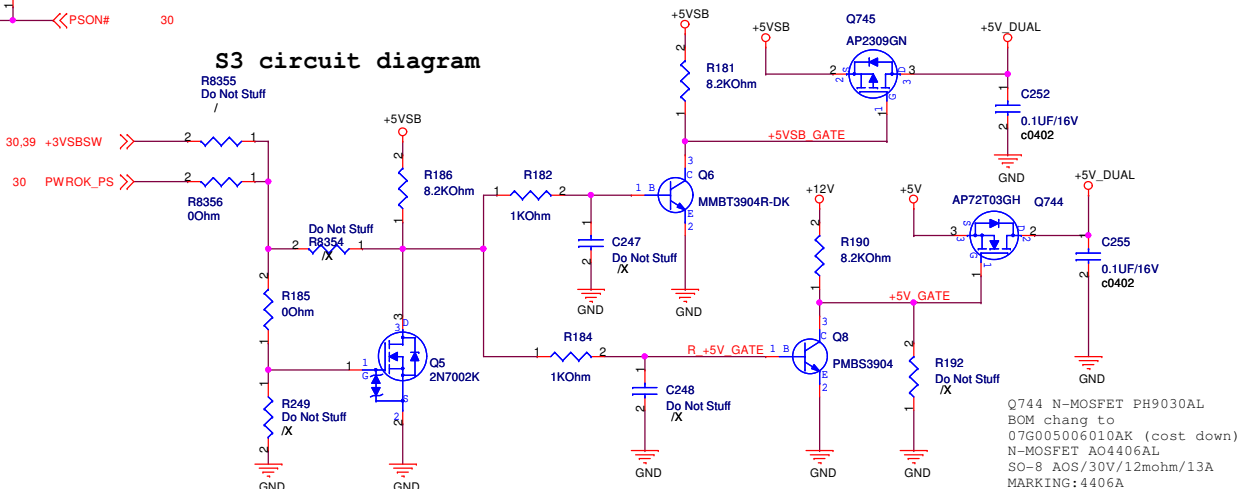


## ATXPWR CONN



\*Around the ATX Power Connector

## S3 circuit diagram



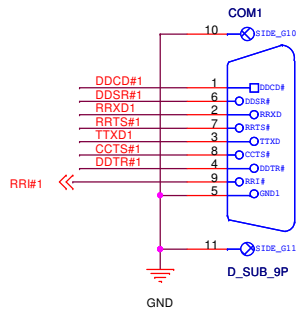
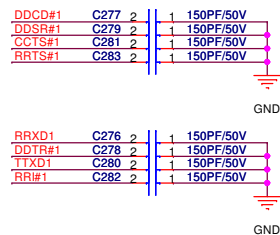
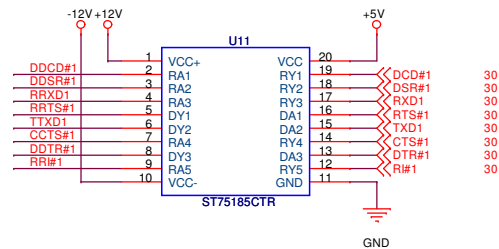
Q744 N-MOSFET PH9030AL  
BOM chang to  
07G005006010AK (cost down)  
N-MOSFET AO4406AL  
SO-8 AOS/30V/12mohm/13A  
MARKING: 4406A

Logic IC : R190 = 2.7K, Q8 = 2N7002  
BJT : R190 = 8.2K, Q8 = 3904, R192  
= uninstall

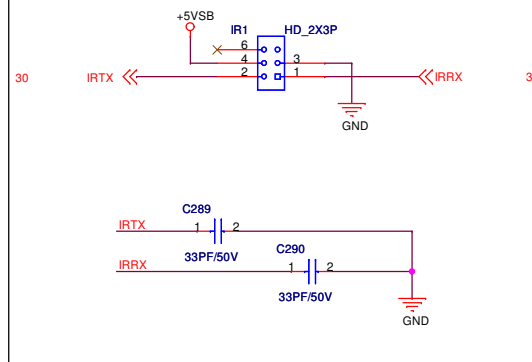
bom

<b>ASRock</b>		Title : <b>POK_DUALSW_ENASUS</b>	
ASRock Inc.		Engineer: <b>Isaac Lee</b>	
Size A3	Project Name <b>H67M-ITX</b>		Rev 1.03
Date: <b>Friday, March 15, 2013</b>		Sheet <b>32</b>	of <b>42</b>

## COM Port



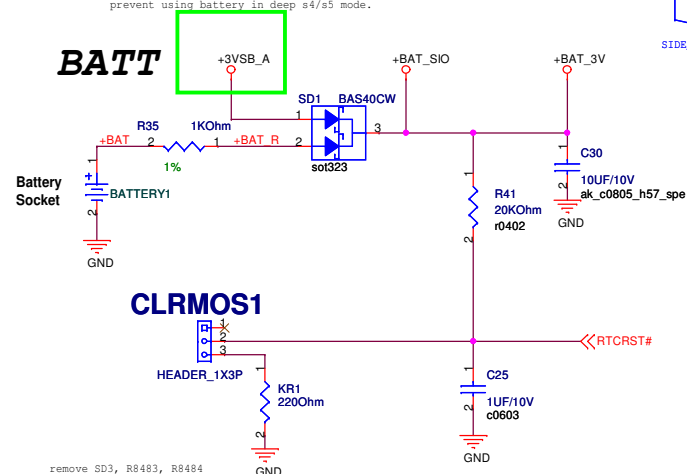
## IR



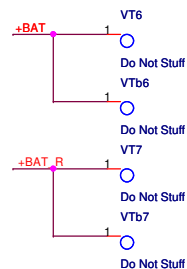
prevent using battery in deep s4/s5 mode.

prevent using battery in deep s4/s5 mode.

## BATT



remove SD3, R8483, R8484

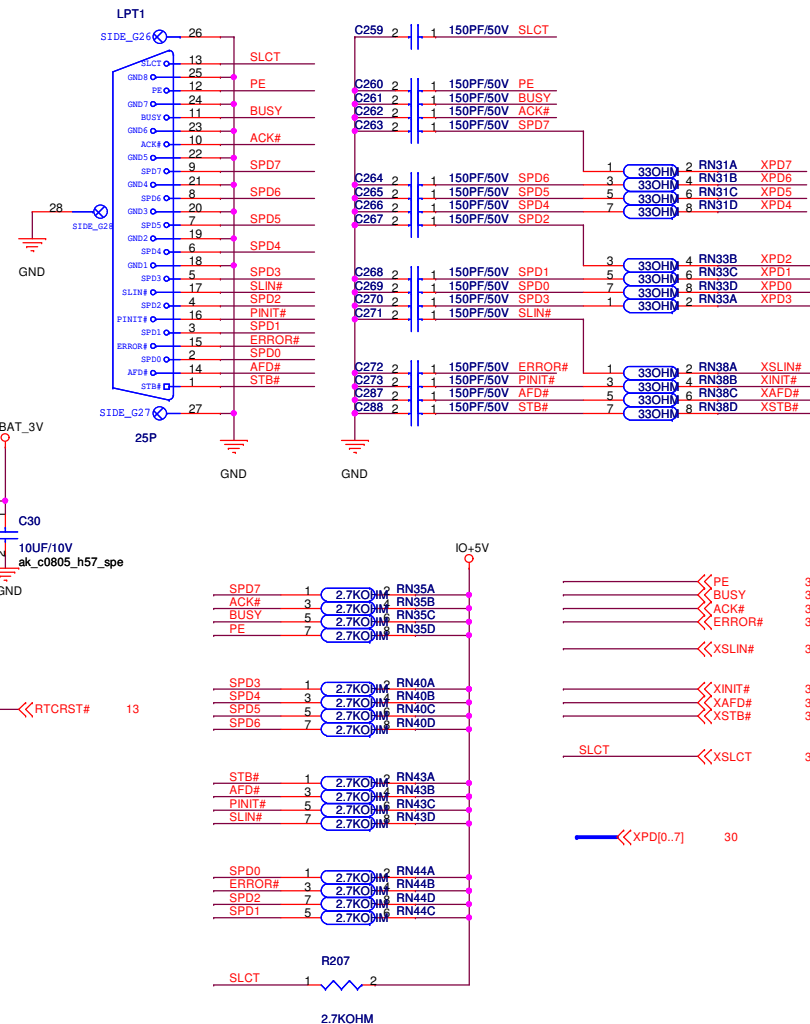


**BATTERY1\_1**  
3V/220mAh



12G044100004

## Parallel Port

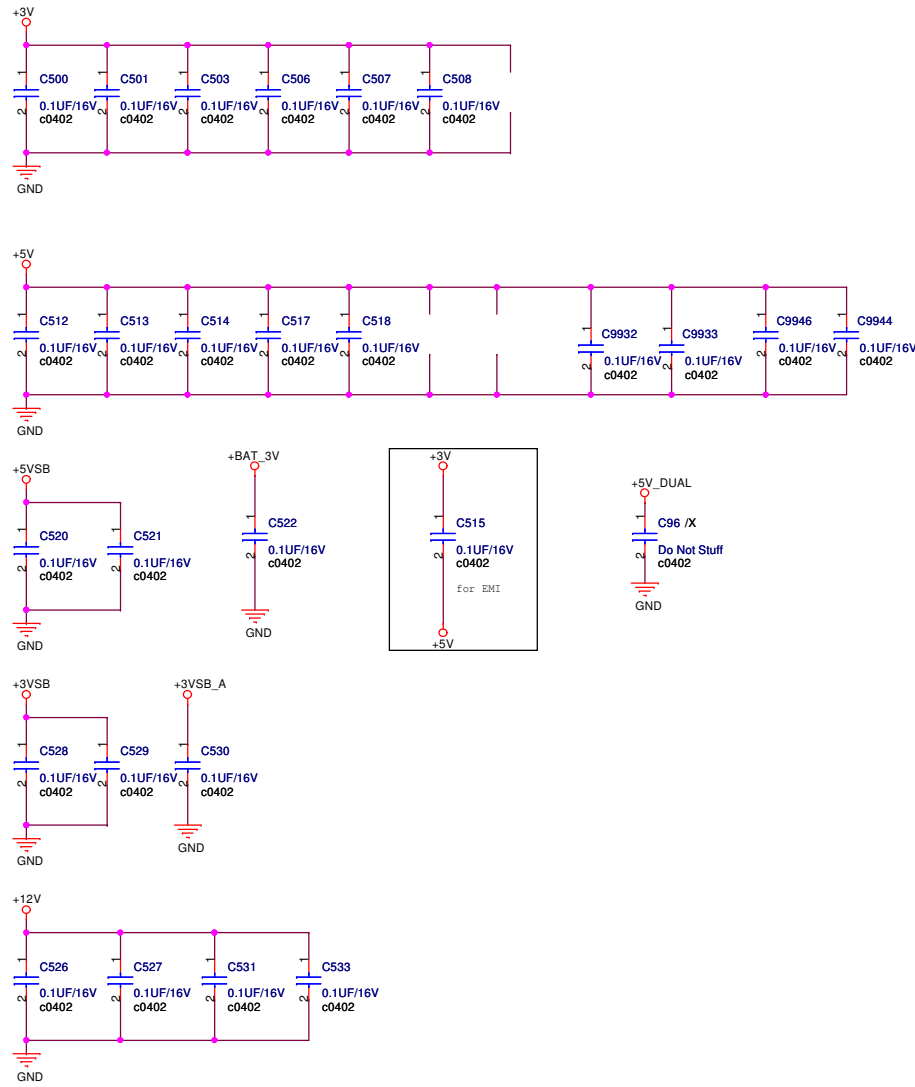
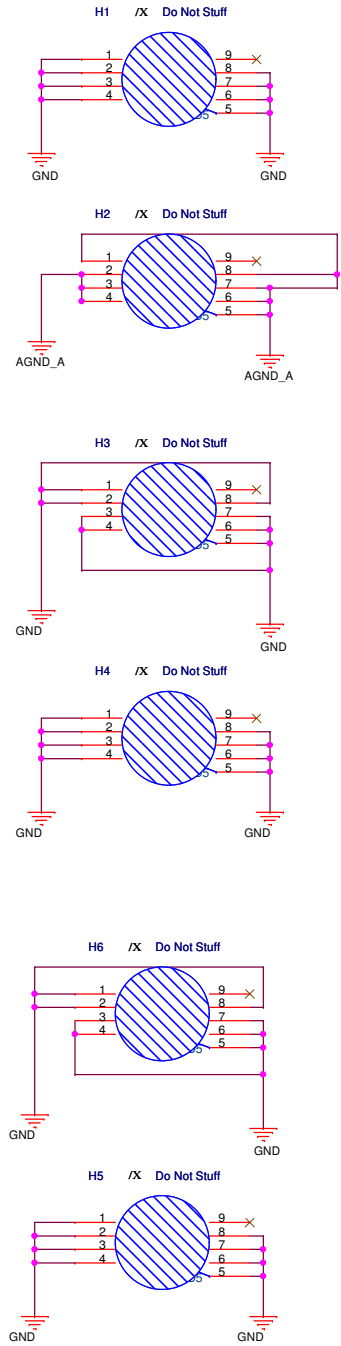


H67M-ITX

ASRock Title : IO CONNECTOR			
ASRock Inc.		Engineer: Isaac Lee	
Size	Project Name	Rev	
A3	H67M-ITX	1.03	
Date: Friday, March 15, 2013	Sheet	33	of 47

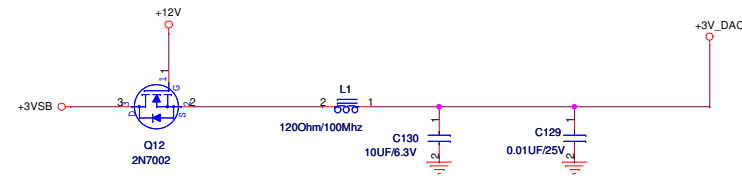


SCREW\_HOLE

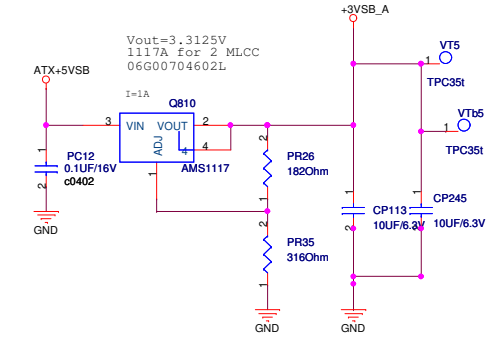


# Soft Start - PCH

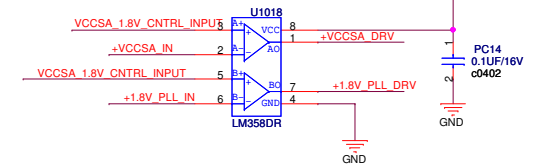
## +3.3V\_DAC



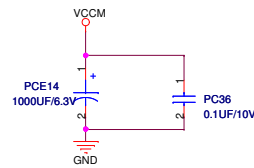
## +3VSB\_A



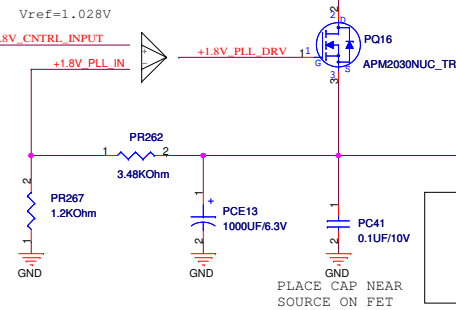
41 +VCCSA\_DRV  
41 +VCCSA\_IN  
41 VCCSA\_1.8V\_CNTRL\_INPUT



CPU\_VTT  
+1.05V\_PCH



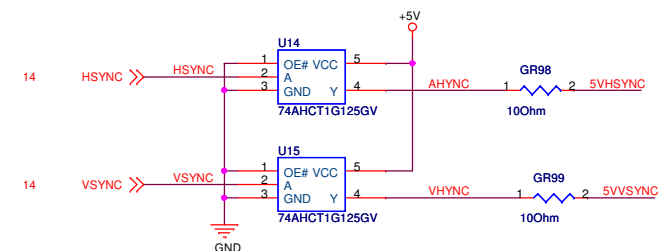
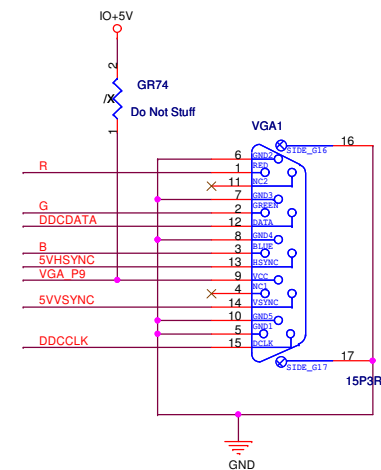
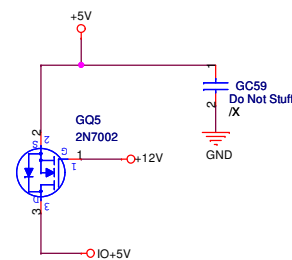
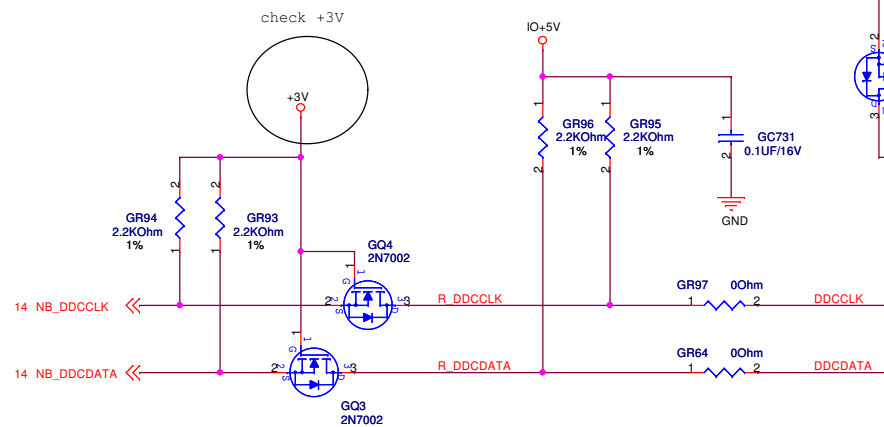
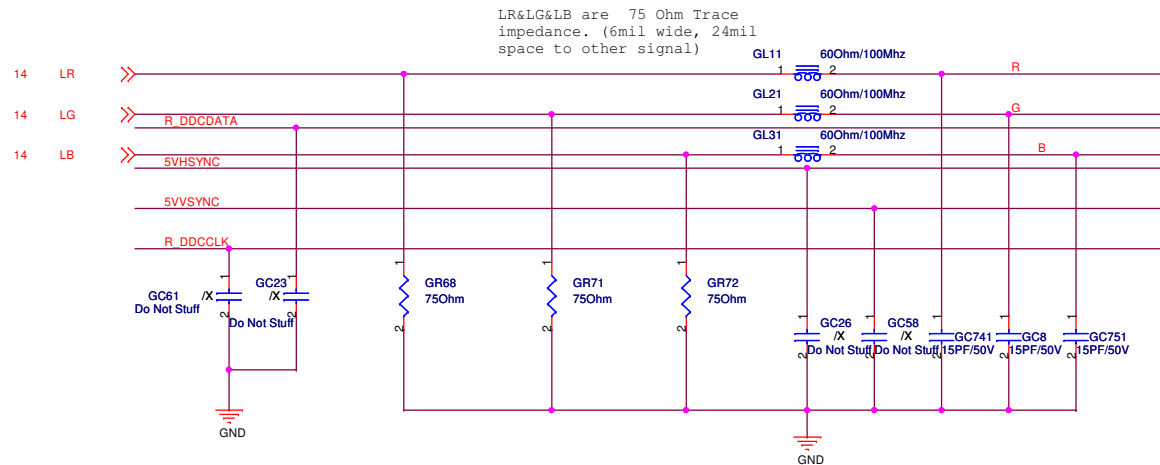
## +1.8V\_PLL Power



PLACE CAP NEAR  
SOURCE ON FET

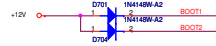
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ASRock™			Title :DC_DC
ASRock Inc.			Engineer: Isaac Lee
Size	Project Name	Rev	
Custom	H67M-ITX	1.03	
Date:	Thursday, March 14, 2013	Sheet	35 of 42



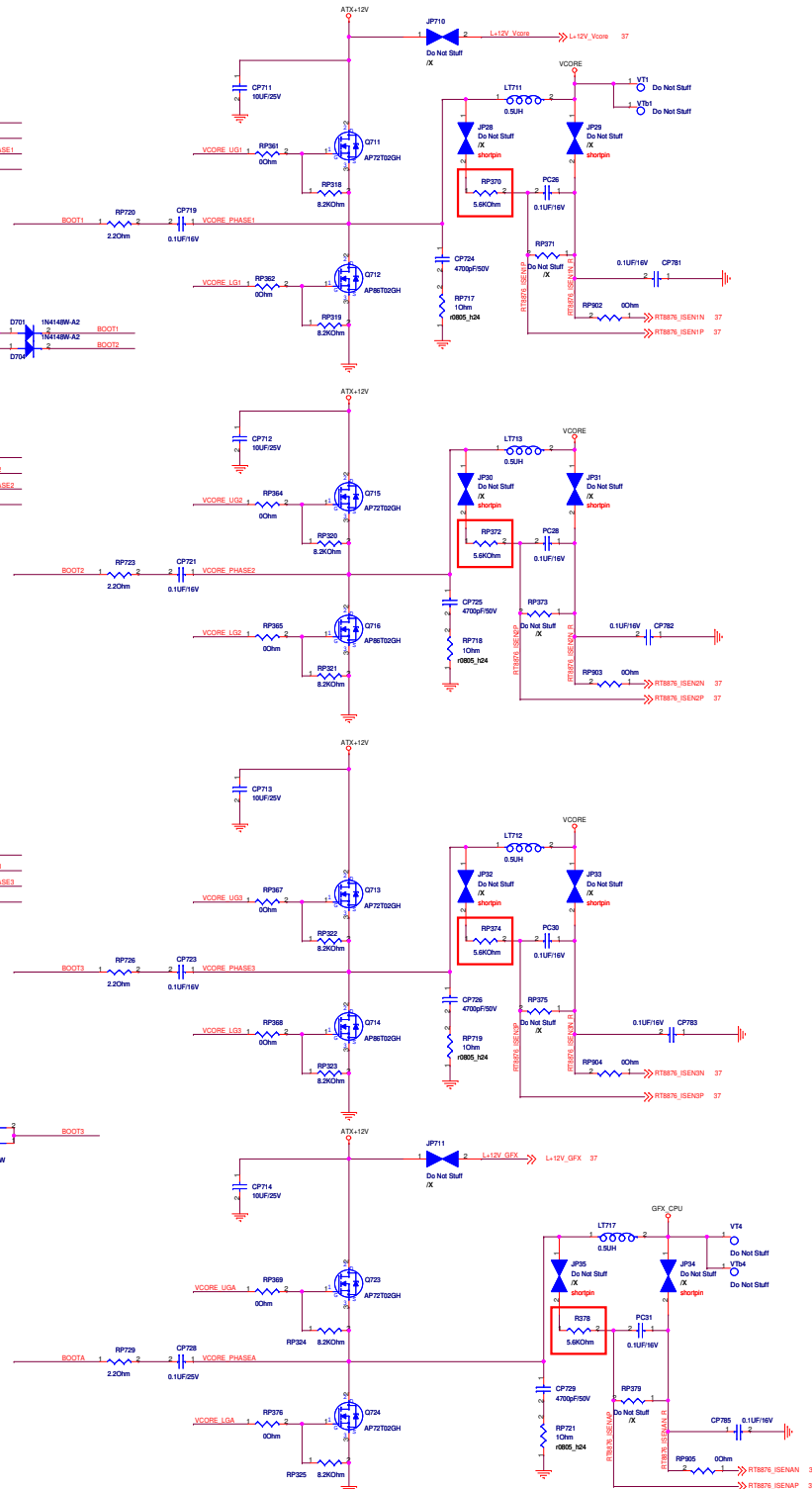
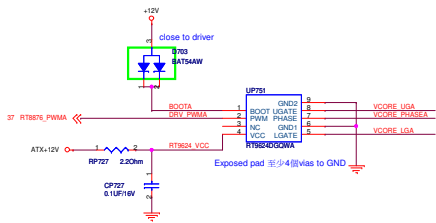
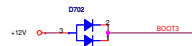
H67M-ITX

37 BOOT1 << BOOT1  
37 VCORE\_LG1 << VCORE\_LG1  
37 VCORE\_PHASE1 << VCORE\_PHASE1  
37 VCORE\_LG1 << VCORE\_LG1

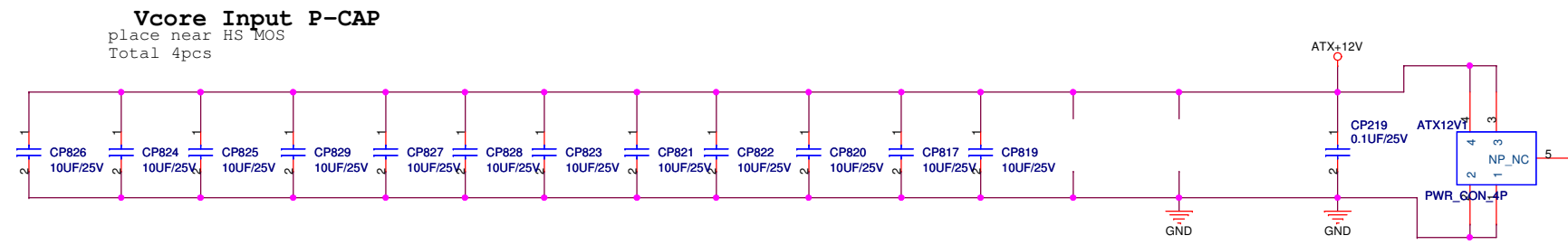
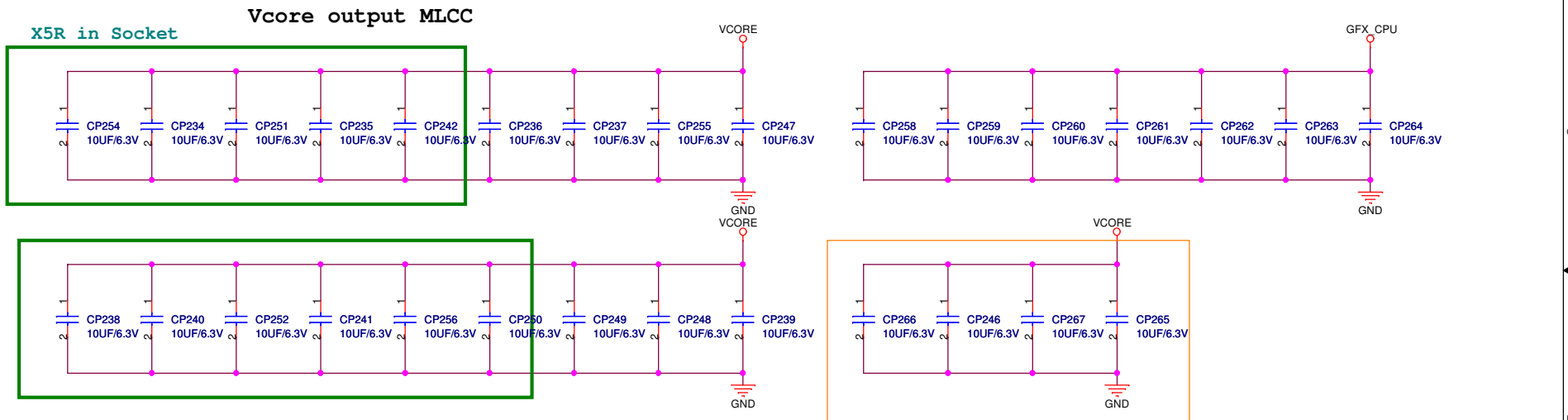
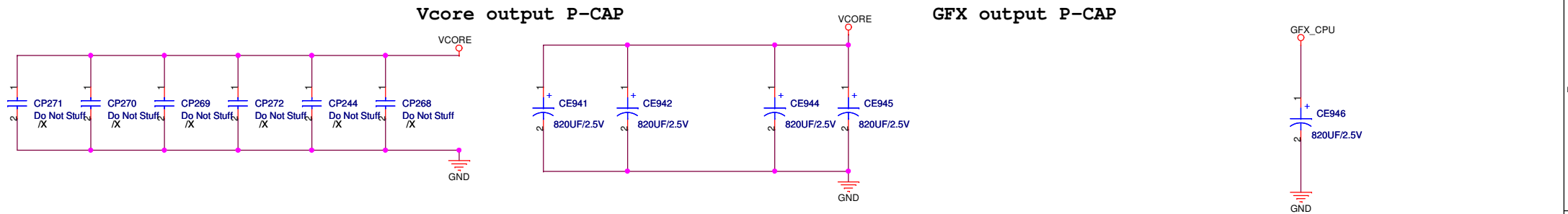


37 BOOT2 << BOOT2  
37 VCORE\_LG2 << VCORE\_LG2  
37 VCORE\_PHASE2 << VCORE\_PHASE2  
37 VCORE\_LG2 << VCORE\_LG2

37 BOOT3 << BOOT3  
37 VCORE\_LG3 << VCORE\_LG3  
37 VCORE\_PHASE3 << VCORE\_PHASE3  
37 VCORE\_LG3 << VCORE\_LG3

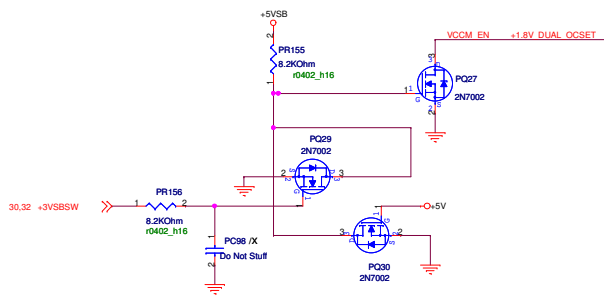






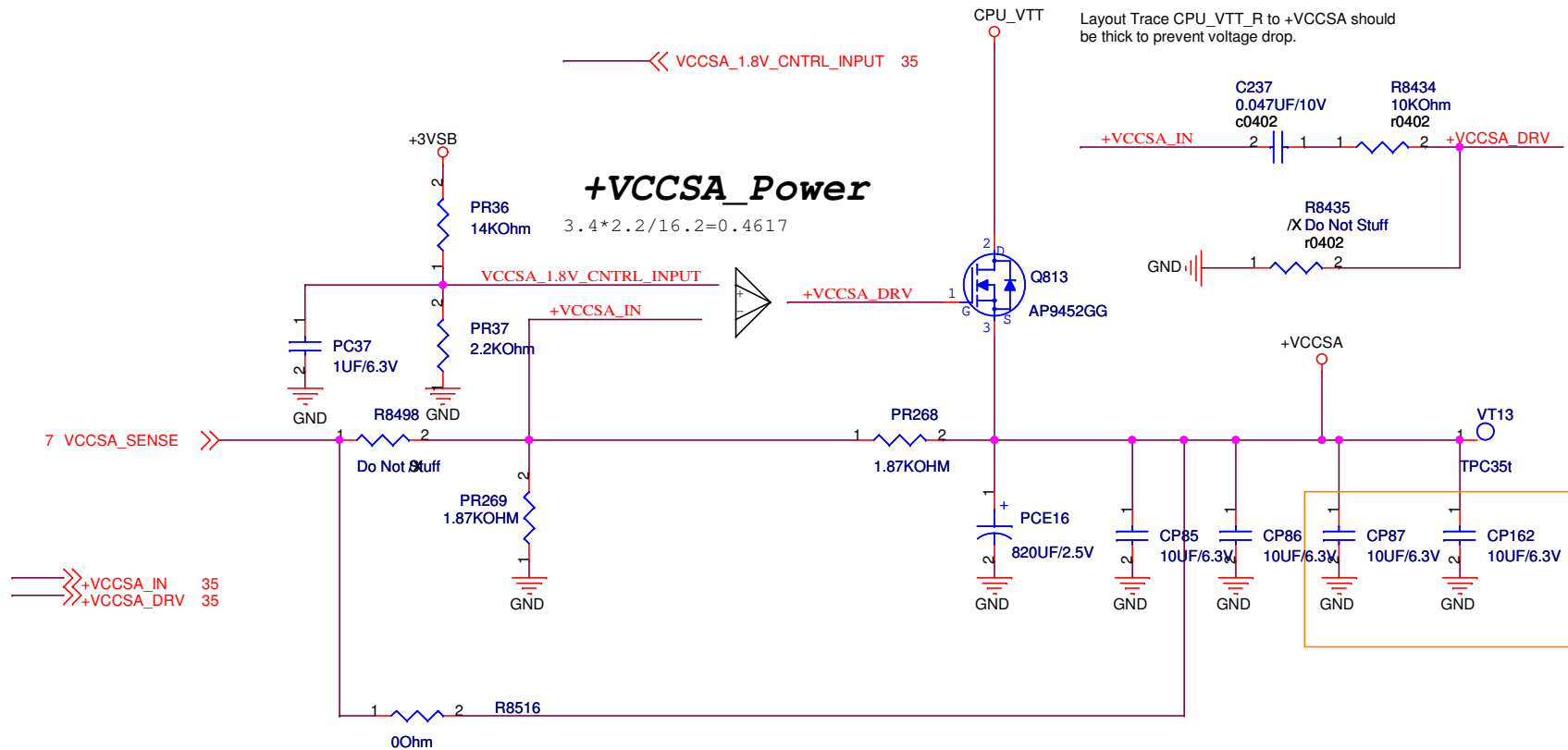
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<b>ASRock</b>		<b>Title : VCORE</b>	
ASRock Inc.		Engineer: Isaac Lee	
Size B	Project Name <b>H67M-ITX</b>		Rev 1.03
Date: Friday, March 15, 2013		Sheet 38	of 42





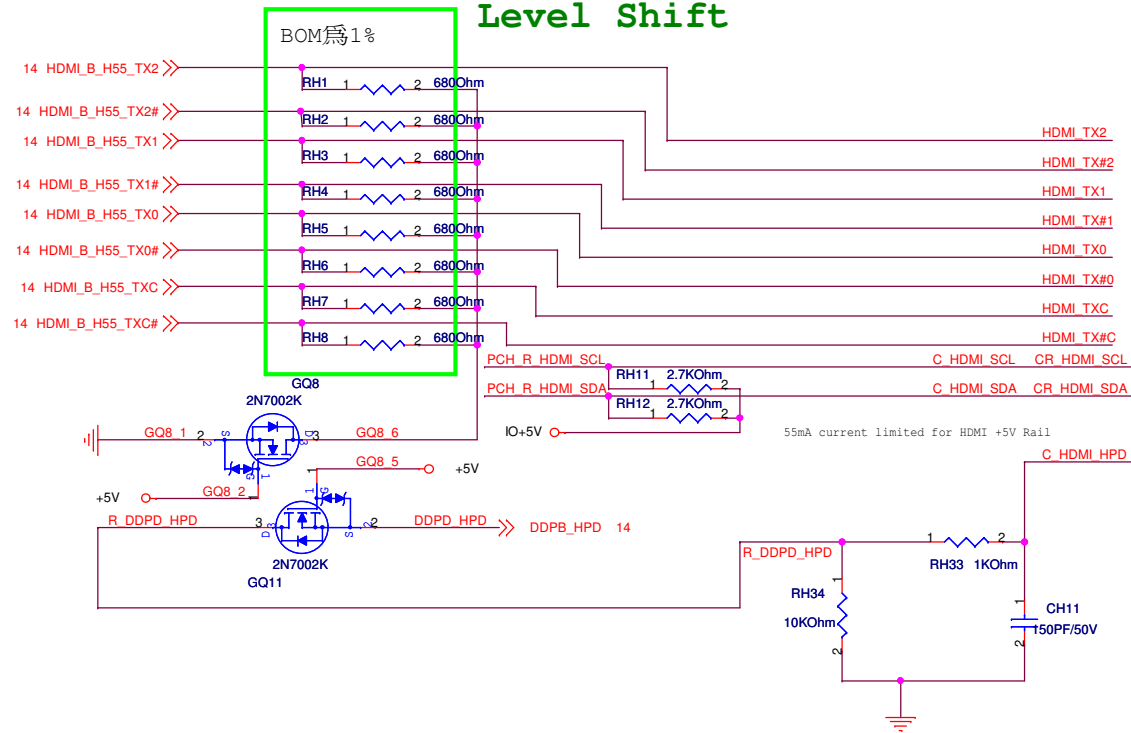




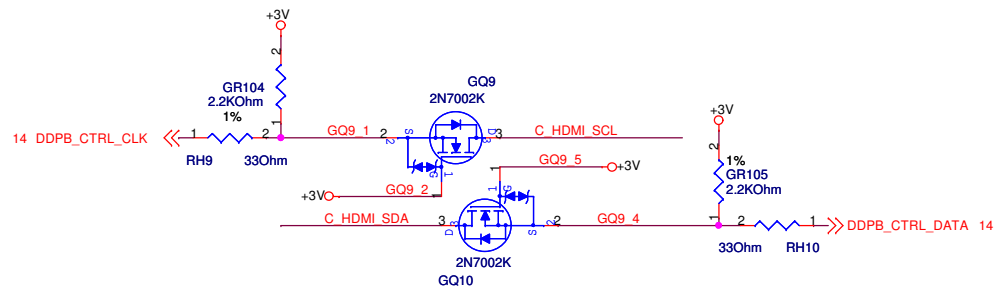
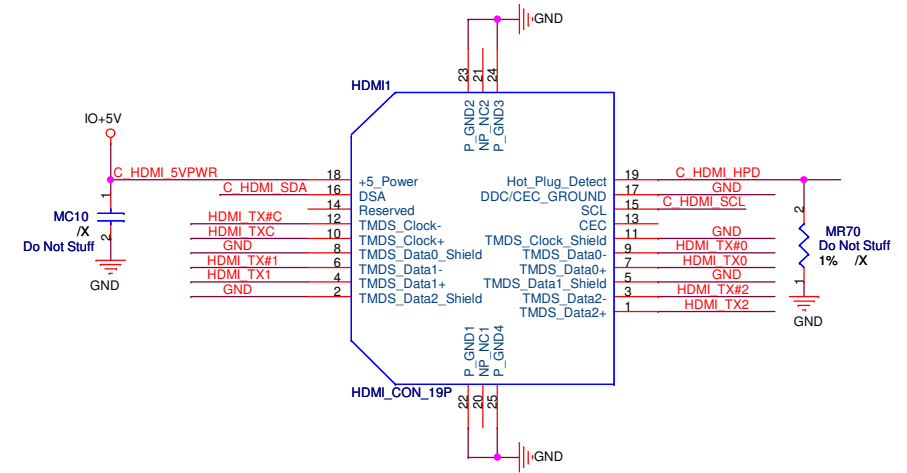
bom

<b>ASRock™</b>		<b>Title : VTT</b>	
ASRock Inc.		Engineer: Chia-Wei Chang	
Size	Project Name		Rev
Custom	<b>H61M-HVS</b>		1.00
Date: Friday, March 15, 2013		Sheet 41 of 42	

## Level Shift



## HDMI CONNECTOR



bom

<b>ASRock</b> Title : <b>HDMI</b>		Engineer: <b>Shih-Hsuan_Chen</b>
Size B	Project Name <b>HM77-HT</b>	Rev 1.02
Date: <b>Friday, March 15, 2013</b>	Sheet <b>42</b> of <b>42</b>	